STIC Search Report
EIC 2800

STIC Database Tracking Number: 129229

TO: Monica Lewis
Location: JEF 5A30
Art Unit : 2822
Wednesday, August 11, 2004

Case Serial Number: 10/065837

From: Irina Speckhard
Location: EIC 2800 JEF 4B59
Phone: (571) 272-2554
irina.speckhard@uspto.gov

Search Notes

Examiner Lewis,

Please find attached prior-art search results from the patent and non-patent abstract and full-text databases. The results were based on claims and statements of technical problems and solutions. Tagged records might be worth your review as well as the rest of the references provided.

If you need further searching or have questions or comments, please let me know.

Thank you,

Irina Speckhard

Date 8/6/04 Serial # 10/063,837 Priority Application Date _____

Your Name M. Lewis Examiner # _____

AU 2899 Phone 272-1838 Room 5A30

In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search, please prioritize in order of need. Need before 8/17 ldb

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

08-06-04 A11:58 IN

Where have you searched so far on this case?
Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____
Secondary Refs ✓ Foreign Patents ___ _____
Teaching Refs ___ _____

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-11

Problem: See paragraphs 4-6
Solution: " " 7-11

Staff Use Only I Heckler Type of Search Vendors

Searcher: _____ Structure (#)_____ STN_____

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EIC2800

Fast & Focused Search Feedback Form

The search results generated for your ***Fast & Focused*** search request are attached.
If you have any questions or comments about the scope or the results of the search, please contact ***the EIC searcher*** who conducted the search ***or contact***:

Jeff.Harrison@uspto.gov , EIC2800 Team Leader, 272-2511

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example: 2810*
- *Were you satisfied with the coverage and search strategies of this search?* ☐ YES ☐ NO

  Why/Why Not?

- *Relevant prior art **found**, search results used as follows:*

  ☐ 102 rejection

  ☐ 103 rejection

  ☐ Cited as being of interest.

  ☐ Helped examiner better understand the invention.

  ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

☐ Foreign Patent(s)

☐ Non-Patent Literature (journal articles, conference proceedings, etc.)

- *Relevant prior art **not found**:*

  ☐ Results verified the lack of relevant prior art (helped determine patentability).

  ☐ Search results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to **STIC-EIC2800, JEF-4B68. Thanks.**

SYSTEM:OS - DIALOG OneSearch
File 2:INSPEC 1969-2004/Aug W1
(c) 2004 Institution of Electrical Engineers
*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 6:NTIS 1964-2004/Aug W2
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(c) 2004 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.
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File 350:Derwent WPIX 1963-2004/UD,UM &UP=200451
(c) 2004 Thomson Derwent
*File 350: For more current information, include File 331 in your search. Enter HELP NEWS 331 for details.
File 347:JAPIO Nov 1976-2004/Apr(Updated 040802)
(c) 2004 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.
File 344:Chinese Patents Abs Aug 1985-2004/May
(c) 2004 European Patent Office
File 371:French Patents 1961-2002/BOPI 200209
(c) 2002 INPI. All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.

Set	Items	Description
S1	7019	(VERTICAL? OR BIPOLAR? OR BI()POLAR?)(3N)(PNP OR NPN OR P(-W)N(W)P OR N(W)P(W)N)
S2	22519	((PNP OR NPN OR P(W)N(W)P OR N(W)P(W)N))(3N)TRANSIST?
S3	6176	VERTICAL?(3N)(NPN OR PNP OR TRANSIST?)
S4	4402	PNP(3N)TRANSIST? AND NPN(3N)TRANSIST?
S5	15403	BICMOS OR BIPOLAR()COMPLEMENTARY()METAL()OXIDE
S6	13134	MC=(U13-D03B2 OR U11-C18A OR U13-D02A)
S7	450952	MOS OR METAL()OXIDE(1W)SEMICONDUCT??????? OR NMOS? ? OR N(-)MOS? ? OR PMOS? ? OR P()MOS? ? OR VMOS? ? OR V()MOS? ? OR C(-)MOS? ? OR CMOS? ? OR NMOSFET? ? OR NMOS()FET? ? OR PMOS()FET? ? OR PMOSFET? ?
S8	116366	DMOS()FET? ? OR DMOSFET? ? OR UMOS()FET? ? OR UMOSFET? ? OR MOS()FET? ? OR MOSFET? ?
S9	172830	(FIELD()EFFECT? ?(1W)TRANSIT???????) OR FET? ?
S10	687823	S1:S9
S11	633436	HIGH?????(3N)PERFORM???????
S12	1476	PERFORM???????(3N)(NPN OR N()P()N OR P()N()P OR PNP)
S13	634514	S11:S12
S14	2586220	SILICON OR SI OR SILICA
S15	71136	POLYSILICON
S16	2600491	S14:S15
S17	323485	GERMANIUM OR GE
S18	127758	SILICON()GERMANIUM OR SIGE OR ((SILICON OR SI) AND (GERMANIUM OR GE))
S19	12158701	CARBON OR "C" OR SIGEC
S20	20198	EMIT?(3N)REGION???
S21	284278	(P OR N)(1N)(TYPE? ? OR EMIT??????)
S22	298984	S20:S21
S23	6454	(EXTRINSIC? OR INTRINSIC?)(3N)BASE?
S24	46504	BASE?(2N)REGION???
S25	51847	S23:S24
S26	23397	S10 AND S13
S27	6963	S26 AND S16
S28	1864	S27 AND (S17 OR S18 OR S19)
S29	257	S28 AND S22
S30	33	S29 AND S25
S31	32	RD (unique items)
S32	224	S29 NOT S30
S33	20	S32 AND S1
S34	20	S33 AND S16
S35	12	RD (unique items)
S36	204	S32 NOT S33
S37	204	S36 AND S22
S38	13	S37 AND S2
S39	10	RD (unique items)
S40	191	S37 NOT S38
S41	16	S40 AND S5
S42	6	RD (unique items)

31/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6795366 INSPEC Abstract Number: B2001-02-2560J-008
Title: 1800 V, 3.8 A bipolar junction transistors in 4H-SiC
Author(s): Sei-Hyung Ryu; Agarwal, A.K.; Singh, R.; Palmour, J.W.
Author Affiliation: Cree Inc., Durham, NC, USA
Conference Title: 58th DRC. Device Research Conference. Conference Digest (Cat. No.00TH8526) p.133-4
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xii+176 pp.
ISBN: 0 7803 6472 4 Material Identity Number: XX-2000-02218
Conference Title: 58th DRC. Device Research Conference
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 19-21 June 2000 Conference Location: Denver, CO, USA
Language: English
Abstract: **Silicon** carbide (SiC) is a very attractive material for high voltage, high power switching devices. Power **MOSFETs** in SiC have received the most attention, but **high performance** SiC **MOSFETs** have yet to be developed due to poor **MOS** mobility and reliability, especially in 4H-SiC. On the other hand, bipolar devices such as GTOs (Agarwal et al, 1999) have demonstrated high blocking voltages and high on-currents, taking full advantage of the material properties of SiC. In this paper, we report the first demonstration of high voltage **NPN bipolar** junction **transistors** in 4H-SiC. The BJTs were able to block 1800 V and showed an on-resistance of 10.8 m Omega cm/sup 2/ (I/sub **C** /=2.7 A at V/sub CE/=2 V for a 1 mm*1.4 mm active area), which outperforms all previously reported SiC power switching devices. Moreover, these transistors show a negative temperature coefficient in the on-resistance characteristics, which enables easy paralleling of the devices. The BJTs were fabricated in 4H-SiC with a 20 mu m thick, 2.5*10/sup 15/cm/sup -3/ doped collector layer, 1 mu m thick, 2.5*10/sup 17/cm/sup -3/ doped base layer, and 0.75 mu m thick **N+ emitter** layer. The **N+ emitter** fingers were isolated by RIE, and then aluminum was implanted to form **base** contact **regions**. The **base** layer was then RIE etched to isolate the devices, and boron ions were implanted to form JTE termination regions. Alloyed Ni was used for both **N-type** and **P-type** ohmic contacts. A Ti/Au layer was then deposited and patterned as overlayer and probing pads.
Subfile: B

31/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

04114187 INSPEC Abstract Number: B9205-2570K-001
Title: Impurity diffusion behavior of bipolar transistor under low-temperature furnace annealing and high-temperature RTA and its optimization for 0.5- mu m Bi-**CMOS** process
Author(s): Norishima, M.; Iwai, H.; Niitsu, Y.; Maeguchi, K.
Author Affiliation: Toshiba Corp., Kawasaki, Japan
Journal: IEEE Transactions on Electron Devices vol.39, no.1 p.33-40
Publication Date: Jan. 1992 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/92/0100-0033$03.00
Language: English

Abstract: A low-temperature-processed (800-850 degrees **C**) bipolar transistor design suitable for the **high-performance** 0.5- mu m **BiCMOS** process is discussed. It has been found that insufficient activation of arsenic in the emitter, enhanced boron diffusion in the low-concentration **base region** . and insufficient arsenic diffusion from the poly **Si** are serious considerations if low-temperature furnace annealing is used. If high-temperature rapid thermal annealing (RTA) is used instead of low-temperature furnace annealing, these problems are resolved. Through impurity diffusion behavior and related electrical bipolar transistor design in the **high-performance** 0. 5- mu m Bi-**CMOS** process are proposed. The As-**P emitter** and selectively implanted collector structures, annealed using RTA, were found to be suitable for the advanced Bi-**CMOS** process.
Subfile: B

31/3,AB/3 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

02656198 Genuine Article#: LU394 Number of References: 18
Title: THEORETICAL SMALL-SIGNAL PERFORMANCE OF **SI/SIGE/SI** HBT (Abstract Available)
Author(s): SANKARAN V; HINCKLEY JM; SINGH J
Corporate Source: N CAROLINA STATE UNIV/RALEIGH//NC/27607; UNIV MICHIGAN,DEPT ELECT ENGN & COMP SCI,CTR HIGH FREQUENCY MICROELECTR/ANN ARBOR//MI/48109
Journal: IEEE TRANSACTIONS ON ELECTRON DEVICES, 1993, V40, N9 (SEP), P 1589-1596
ISSN: 0018-9383
Language: ENGLISH Document Type: ARTICLE
Abstract: We have applied the Monte Carlo technique to analyze electron and hole transport in bulk Si0.8Ge0.2 and strained Si0.8Ge0.2//**Si**. The computed minority- and majority-carrier transport properties were used in a comprehensive small-signal model to evaluate the **high**-frequency **performance** of a state-of-the-art **n-p-n** heterostructure **bipolar transistor** (HBT) fabricated with **SiGe** as the base material. The valence band discontinuity of a **SiGe**-base HBT reverses the degradation in emitter injection efficiency caused by bandgap narrowing in the base, and permits a higher ratio of base doping to emitter doping than would be practical for a bipolar transistor. Any degradative effect of increased base doping on electron and hole mobilities is off set by improved transport in the strained **SiGe** base, resulting in a marked decrease in the base resistance and base transit time. Compared to the **Si** BJT, the use of Si0.8Ge0.2 for the **base region** of an HBT leads to significant improvements in low-frequency common emitter current gain h(fe)(0), low-frequency unilateral power gain U(0), and maximum oscillation frequency f(max). The transition frequency f(T) also improves, but not to such a degree.

31/3,AB/4 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

01813033 Genuine Article#: JC979 Number of References: 32
Title: COMPARATIVE-ANALYSIS OF THE **HIGH**-FREQUENCY **PERFORMANCE** OF **SI**/SI1-XGEX HETEROJUNCTION BIPOLAR AND **SI**

BIPOLAR-TRANSISTORS (Abstract Available)
Author(s): CHEN J; GAO GB; MORKOC H
Corporate Source: INTEL CORP,PORTLAND TECHNOL DEV,AL4-76,5200 NE ELAM YOUNG PKWY/HILLSBORO//OR/97124; UNIV ILLINOIS,COORDINATED SCI LAB/URBANA//IL/61801; UNIV ILLINOIS,MAT RES LAB/URBANA//IL/61801
Journal: SOLID-STATE ELECTRONICS, 1992, V35, N8 (AUG), P1037-1044
Language: ENGLISH Document Type: ARTICLE
Abstract: This paper presents a model-based comparison of the **high**-frequency **performance** of **Si**/Si1-xGex heterojunction bipolar transistors (HBTs) and **Si** bipolarjunction transistors (BJTs), in which the structural parameters were designed for maximum f(T) almost-equal-to f(max). This model study shows: (1) the Si1-xGex HBT has a peak f(T)(=f(max)) of 64 GHz, which represents a 16.4% improvement over the **Si** BJT; (2) emitter charging time has a sizable effect on **high**-frequency **performance**, even at current densities as high as 80 kA cm-2; (3) compositional grading of the **SiGe** base, as well as the profile of the base doping, strongly influence f(T) and f(max). A Gaussian grading profile is found to exhibit the highest peak f(T)=f(max); a 30% higher peak cutoff frequency is predicted over a uniform doping profile; (4) the dependence of **high**-frequency **performance** upon collector design represents a trade-off between f(T), f(max) and BV(CBO); and (5) by decreasing emitter or base doping levels, Si1-xGexHBTs with f(T) exceeding 100 GHz can be designed. Alternatively, f(max) of 100 GHz may be achieved by increasing **base** doping and reducing **extrinsic** capacitances and resistances.

31/3,AB/5 (Item 3 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

01385393 Genuine Article#: GV120 Number of References: 20
Title: IMPURITY DIFFUSION BEHAVIOR OF BIPOLAR-TRANSISTOR UNDER LOW-TEMPERATURE FURNACE ANNEALING AND HIGH-TEMPERATURE RTA AND ITS OPTIMIZATION FOR 0.5-MU-M BI-**CMOS** PROCESS (Abstract Available)
Author(s): NORISHIMA M; IWAI H; NIITSU Y; MAEGUCHI K
Corporate Source: TOSHIBA CO LTD,SEMICOND DEVICE ENGN LAB,1 KOMUKAI TOSHIBA CHU,SAIWAI KU/KAWASAKI 210//JAPAN/; TOSHIBA CO LTD,ULSI RES CTR,SAIWAI KU/KAWASAKI 210//JAPAN/
Journal: IEEE TRANSACTIONS ON ELECTRON DEVICES, 1992, V39, N1, P33-40
Language: ENGLISH Document Type: ARTICLE
Abstract: A low-temperature-processed (800-850-degrees-**C**) bipolar transistor design suitable for the **high-performance** 0.5-mu-m Bi-**CMOS** process is discussed. It has been found that insufficient activation of arsenic in the emitter, enhanced boron diffusion in the low-concentration **base region**, and insufficient arsenic diffusion from the poly **Si** are serious considerations, if low-temperature furnace annealing is used. If high-temperature RTA is used instead of low-temperature furnace annealing, these problems are resolved. Through impurity diffusion behavior and related electrical bipolar characteristics, the optimum conditions and structures for bipolar transistor design in the **high-performance** 0.5-mu-m Bi-**CMOS** process are proposed. It was shown that the minimum W(B) was limited by BV(CEO) and BV(EBO). The As-**P emitter** and SIC structures, annealed RTA, were found to be suitable for the advanced Bi-**CMOS** process.

31/3,AB/6 (Item 1 from file: 350)

DIALOG(R)File 350:Derwent WPIX

016309380
WPI Acc No: 2004-467275/200444
XRAM Acc No: C04-174969
XRPX Acc No: N04-369169
Heterojunction bipolar transistor used in electronic application such as integrated circuits and discrete components, comprises semiconductor substrate having first region containing first dopant for forming **base region**
Patent Assignee: SEMICONDUCTOR COMPONENTS IND LLC (SEMI-N)
Inventor: LOECHELT G H
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040106264	A1	20040603	US 2002307590	A	20021202	200444	B
DE 10352765	A1	20040609	DE 10352765	A	20031112	200444	
JP 2004186675	A	20040702	JP 2003373787	A	20031031	200444	
US 6764918	B2	20040720	US 2002307590	A	20021202	200448	

Priority Applications (No Type Date): US 2002307590 A 20021202
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040106264	A1		9	H01L-031/328	
DE 10352765	A1			H01L-029/73	
JP 2004186675	A		10	H01L-021/331	
US 6764918	B2			H01L-021/76	

Abstract (Basic): US 20040106264 A1
Abstract (Basic):
NOVELTY - An **NPN** heterojunction **bipolar transistor** (HBT) has semiconductor substrate (11) having first region containing first dopant for forming **base region** (12) of transistor and second region adjacent to first region that includes an interstitial trapping material.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:
(1) a semiconductor device comprising semiconductor substrate having surface formed with dielectric material (32), first semiconductor layer formed adjacent to the dielectric material and including interstitial trapping material, and second semiconductor layer doped to form a **base region** of the semiconductor device; and
(2) a method of forming NPN HBT comprising providing the semiconductor substrate having first region and second region.
USE - Used in electronic application such as integrated circuits and discrete components.
ADVANTAGE - The invention has narrow base doping profile providing superior **high** frequency **performance**.
DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of the NPN HBT after a third fabrication stage.
Semiconductor substrate (11)
Base layer (12)
Epitaxial layer (13)
Buried layer (14)
Trenches (17)
Dielectric layer (18)
Dielectric material (32)
Semiconductor device (100)
pp; 9 DwgNo 4/5

31/3,AB/7 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016281833
WPI Acc No: 2004-439728/200441
XRAM Acc No: C04-164634
XRPX Acc No: N04-347982
Integrated circuit for receiver circuit in wireless communications devices, has substrate with surface doped to form first **base region**, and conductive spacers along first opening sidewalls to define **emitter** and collector **regions**
Patent Assignee: SEMICONDUCTOR COMPONENTS IND LLC (SEMI-N)
Inventor: AZAM M; COSTA J C; LOECHELT G H; MORGAN J R; ZDEBEL P J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040099896	A1	20040527	US 2002303168	A	20021125	200441	B

Priority Applications (No Type Date): US 2002303168 A 20021125
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040099896	A1		9	H01L-027/108	

Abstract (Basic): US 20040099896 A1
Abstract (Basic):
NOVELTY - An integrated circuit comprises a substrate with a surface doped to form a first **base region**, a film formed on the substrate with a first opening over an edge of the **base region**, a first conductive spacer along a first sidewall of the first opening to define a first **emitter region** in the **base region**, and a second conductive spacer formed on the surface along a second sidewall of the first opening to define a first collector region.
USE - The integrated circuit is used for receiver circuits in wireless communications devices.
ADVANTAGE - The assembly provides both **high performance** **NPN** and **PNP transistors** and can be manufactured at a low cost.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of an integrated circuit.
NPN transistor (10)
Substrate (11)
PNP transistor (20)
Collectors (26, 27)
Base region (30)
pp; 9 DwgNo 1/4

31/3,AB/8 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016281832
WPI Acc No: 2004-439727/200441
XRAM Acc No: C04-164633
XRPX Acc No: N04-347981
Vertical transistors for bi-complementary **metal**

oxide semiconductor device used in mobile communications, includes single **silicon** layer that forms **emitter region**, and **extrinsic** and **intrinsic base regions**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: GRAY P B; JOHNSON J B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040099895	A1	20040527	US 200265837	A	20021125	200441	B

Priority Applications (No Type Date): US 200265837 A 20021125
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040099895	A1		21	H01L-027/108	

Abstract (Basic): US 20040099895 A1
Abstract (Basic):

NOVELTY - **Vertical** PNP (sic) and **NPN** (sic) **transistors** comprises a single **silicon** layer that forms an **emitter** (64) **region** of the **PNP transistor**, and an **extrinsic base region** (62) of the **NPN transistor** and an **intrinsic base region** (63) of the **NPN transistor.**

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of forming a **PNP transistor** while forming a complementary **metal oxide semiconductor** device and an **NPN transistor**, comprising a first masking step that defines a first opening through which implants for an **intrinsic base** and a collector of the **PNP transistor** are made, and a second masking step that defines an emitter of the **PNP transistor.**

USE - For bi-complementary **metal oxide semiconductor** device used in mobile communications.

ADVANTAGE - The transistor exhibits **high performance.**

DESCRIPTION OF DRAWING(S) - The figure shows the resulting **high performance NPN** and **PNP transistor.**

Polysilicon layer (38)
Silicon and **germanium** (46)
Extrinsic base region (62)
Intrinsic base region (63)
Emitter (64)
pp; 21 DwgNo 16/16

31/3,AB/9 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015634694
WPI Acc No: 2003-696876/200366
XRAM Acc No: C03-191451
XRPX Acc No: N03-556564
Integrated circuit fabricated in semiconductor material of first conductivity type, and having **vertical** bipolar **transistor**(s) comprises layer of opposite conductivity type buried in semiconductor material of first conductivity type
Patent Assignee: SALLING C T (SALL-I); WU Z (WUZZ-I); TEXAS INSTR INC (TEXI)
Inventor: SALLING C T; WU Z
Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030137029	A1	20030724	US 200251639	A	20020118	200366	B
US 6724050	B2	20040420	US 200251639	A	20020118	200427	

Priority Applications (No Type Date): US 200251639 A 20020118

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030137029	A1		10	H01L-027/82	
US 6724050	B2			H01L-023/62	

Abstract (Basic): US 20030137029 A1

Abstract (Basic):

NOVELTY - An integrated circuit (300) fabricated in semiconductor material (301) of a first conductivity type, the circuit having at the surface a **vertical** bipolar **transistor**(s) comprises:

(i) a layer of the opposite conductivity type buried in the semiconductor material of the first conductivity type, as collector of the transistor having sharp junctions; and

(ii) a subsurface semiconductor band of the first conductivity type

DETAILED DESCRIPTION - An integrated circuit fabricated in semiconductor material of a first conductivity type, the circuit having at the surface a **vertical** bipolar **transistor**(s) surrounded at least in part by a dielectric isolation zone, comprises:

(a) a first surface region of opposite conductivity type, as an emitter(310, 311);

(b) a second surface region of the first conductivity type, as a base contact (312, 313);

(**c**) a well (371) of opposite conductivity type surrounding the first and second surface regions, extending from the surrounding deep into the semiconductor material of the first conductivity type;

(d) a layer of the opposite conductivity type buried in the semiconductor material of the first conductivity type, as collector of the transistor having sharp junctions;

(e) a subsurface semiconductor band of the first conductivity type between the layer and the surface and surrounded by the well, the band being the base of the transistor providing a width controlled, by the proximity of the buried layer (360) junction to the surface, and a resistivity higher than the remainder of the semiconductor material, thus enabling the **vertical** bipolar **transistor** to operate as a low breakdown voltage transistor for low electrostatic discharge (ESD) clamping voltage and high-beta.

The layer extends laterally to the wells, electrically isolating the base and emitter portions of the transistor from the remainder of the semiconductor material. It extends vertically from the surface regions, beginning at a level more shallow than the depth of the dielectric isolation zone, and extending to a depth greater than the depth of the dielectric zone.

An INDEPENDENT CLAIM is also included for a method of fabricating, in a semiconductor region of a first conductivity type having two wells of the opposite conductivity type, a **vertical** bipolar **transistor**, comprising:

(1) depositing a photoresist layer (330), over the surface of the region and opening a window (330a) in the layer, exposing the surface area between the wells;

(2) implanting at low energy ions of the opposite conductivity type through the window, creating a shallow layer of the opposite conductivity under the surface; and

(3) implanting, at high energy and high dose (340), ions of the opposite conductivity type into the region of the first conductivity

type through the window, creating a deep buried region having a net doping of the opposite conductivity type between, and connecting to the wells, as the collector of the transistor, and further creating a near-surface region of the first conductivity type, having a doping concentration lower than that of the remainder of the **region**, being the **base** of the transistor.

USE - Used as integrated circuit, e.g. **metal-oxide-semiconductor** integrated circuits, useful in electronic systems.

ADVANTAGE - The method is coherent and of low-cost, enhancing ESD insensitivity without the need for additional, real-estate consuming protection devices. It is simple, yet flexible enough for different semiconductor product families and a wide spectrum of design and process variations. The device structure provides for excellent electrical **performance**, mechanical stability and **high** reliability. No investment in new manufacturing machines is needed. The substrate resistance is increased as a welcome side effect of the fabrication of the collector by ion implantation. The collector has a low breakdown voltage, and thus low ESD clamping voltage. A **silicon** area-saving **vertical transistor**, is created, without an additional photomask step.

DESCRIPTION OF DRAWING(S) - The figure is a schematic cross section of a **vertical** bipolar **transistor** with buried collector.

Integrated circuit (300)
Semiconductor material (301)
Inner pair (302)
Emitter (310, 311)
Base contact (312, 313)
Photoresist layer (330)
Window (330a)
High energy and high dose (340)
Buried layer (360)
Outer pair (370)
Wells (371)
pp; 10 DwgNo 3/3

31/3,AB/10 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015564288
WPI Acc No: 2003-626444/200359
XRAM Acc No: C03-171174
XRPX Acc No: N03-498510
Bipolar transistor in integrated circuit includes heterojunction base region disposed, **intrinsic emitter region**, collector **region**, **polysilicon base** electrode with filament, insulating film, and emitter and collector plugs
Patent Assignee: BABCOCK J A (BABC-I); HOWARD G E (HOWA-I); PINTO A (PINT-I)
Inventor: BABCOCK J A; HOWARD G E; PINTO A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030122154	A1	20030703	US 2001342267	P	20011227	200359	B
			US 2002313349	A	20021206		

Priority Applications (No Type Date): US 2001342267 P 20011227; US 2002313349 A 20021206
Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes
US 20030122154 A1 12 H01L-031/328 Provisional application US 2001342267

Abstract (Basic): US 20030122154 A1
Abstract (Basic):
NOVELTY - A bipolar transistor in an integrated circuit comprises a heterojunction **base region** disposed in a single-crystal semiconductor layer, an intrinsic **emitter region** adjacent to the **base region**, a collector **region** adjacent the **base region**, a **polysilicon base** electrode having a filament contacting the **base region**, an insulating film, and emitter plug and collector plug.

DETAILED DESCRIPTION - A bipolar transistor in an integrated circuit comprises a heterojunction **base region** (20) positioned in a single-crystal semiconductor layer, an intrinsic **emitter region** disposed in the semiconductor layer adjacent to the **base region**, a collector **region** adjacent the **base region**, a **polysilicon base** electrode overlying at least a portion of the collector region and having a filament contacting the **base region**, an insulating film disposed between the base electrode and the portion of the collector **region** underlying the **base** electrode, an emitter plug contacting the **emitter region** (25), and a collector plug (24c, 24e) contacting the collector region (28).

An INDEPENDENT CLAIM is also included for a method of fabricating the heterojunction bipolar transistor in a single-crystal **silicon** layer overlying an insulator layer (8).

USE - Used as a bipolar transistor in an integrated circuit, e.g. bi-complementary metal oxide (**BiCMOS**) and **BiCMOS** integrated circuit.

ADVANTAGE - The assembly provides **higher** frequency power **performance** that conventional transistor, and eliminates the need for a highly doped buried layer that can cause problems when epitaxial deposits are used in a standard **vertical transistor**. It also provides high cutoff frequency and excellent switching performance.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a heterojunction bipolar transistor.

Insulator layer (8)
Insulating filament (12)
Base region (20)
Collector plug (24c, 24e)
Emitter region (25)
Collector region (28)
pp; 12 DwgNo 1/3

31/3,AB/11 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010400818
WPI Acc No: 1995-302131/199539
XRAM Acc No: C95-135287
XRPX Acc No: N95-229376
Bi-**CMOS** compatible bipolar transistor - having a laterally graded emitter and self-alignment of emitter and base contacts
Patent Assignee: VLSI TECHNOLOGY INC (VLSI-N)
Inventor: LOH Y; WANG C S; YU H
Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5444003	A	19950822	US 9381761	A	19930623	199539	B

Priority Applications (No Type Date): US 9381761 A 19930623

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5444003	A		19	H01L-021/265	

Abstract (Basic): US 5444003 A

Process for making a bipolar transistor (4) having reduced hot-carrier generation and self-aligning emitter and base contacts, comprises: (a) forming, above a region, B of the substrate whereon a base will be formed, a poly-**Si** conductor doped with a dopant of first conductivity type (CT); (b) implanting a dopant of first CT into substrate regions overlying regions, E, wherein a lateral emitter will be formed; (c) driving-in the said dopant from poly-**Si** conductor into region and driving in said dopant from substrate into region E thereby forming an **extrinsic base region** and a **base**-link **region**; (d) implanting a dopant of second CT into regions E; (c) forming spaced-out sidewall spacers overlying at least a part of region E, the spacers spaced apart by a distance defining a **region** where an active **emitter** will be formed, bounded by lateral **emitter regions**; (f) implanting a dopant of first CT region between sidewall spacers to form an **intrinsic base region**, B; (g) implanting a dopant of second CT having higher impurity concn than the implantation of step (b), to form an active **emitter region** of higher dopant concn than lateral **emitter regions**; (h) forming an external base contact coupled to the polymer-**Si** conductive overlying **extrinsic base regions**; and (i) providing an external emitter contact to the active **emitter region** of the bipolar transistor.

USE - Used in **BiCMOS** integrated circuit mfr.

ADVANTAGE - The bipolar transistor has a laterally graded emitter that reduces generation of hot carriers and the sidewall spacers permit self-alignment and hence smaller geometry and improved **high**-frequency **performance**. May be fabricated simultaneously with **CMOS** device.

Dwg.6,8A/8

31/3,AB/12 (Item 7 from file: 350)

DIALOG(R)File 350:Derwent WPIX

009579577

WPI Acc No: 1993-273123/199334

XRAM Acc No: C93-121863

XRPX Acc No: N93-209742

Mfr. of complementary bipolar **polysilicon@** emitter devices on a single substrate - involves depositing single **polysilicon@** layer on substrate, forming complementary transistors by etching ring-like slots around bipolar emitter areas, filling with insulating oxide etc.

Patent Assignee: ANALOG DEVICES INC (ANLG)

Inventor: KRIEGER W A; MARTINEZ A M; MCDEVITT M R; ROBINSON D W

Number of Countries: 019 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9316494	A1	19930819	WO 93US816	A	19930129	199334	B
US 5409845	A	19950425	US 92828745	A	19920131	199522	

			US 93119890	A	19930910	
US 5444285	A	19950822	US 92828745	A	19920131	199539
			US 92991217	A	19921215	
			US 93120137	A	19930910	
			US 94337148	A	19941109	
US 5541120	A	19960730	US 92828745	A	19920131	199636
			US 93119890	A	19930910	
			US 94337154	A	19941109	

Priority Applications (No Type Date): US 92828745 A 19920131; US 93119890 A 19930910; US 92991217 A 19921215; US 93120137 A 19930910; US 94337148 A 19941109; US 94337154 A 19941109

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9316494	A1	E	46	H01L-027/06	
Designated States (National): CA JP					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
US 5409845	A		15	H01L-021/265	Cont of application US 92828745
US 5444285	A		15	H01L-029/04	Div ex application US 92828745
					Cont of application US 92991217
					Cont of application US 93120137
US 5541120	A			H01L-021/265	Cont of application US 92828745
					Cont of application US 93119890
					Cont of patent US 5409845

Abstract (Basic): WO 9316494 A

Formation of an IC structure comprises (a) depositing a **polysilicon** layer on a **Si** substrate; (b) forming an insulating isolation ring within the above layer and surrounding **regions** where an **emitter** is to be formed; (c) forming a self-aligned emitter within the substrate below inside regions of the **polysilicon**; and (d) forming a **base** contacting **region** within the substrate, below the outside regions of the **polysilicon**.

Also claimed is the mfr. of an IC structure including at least one bipolar transistor and at least one **MOSFET** on a substrate, comprising; (i) defining buried layers in the substrate; (ii) forming bipolar doped **intrinsic base region** in the substrate; (iii) following steps (a)-(d) above; (iv) forming **MOS** gates; (v) forming **MOS** source and drain regions; (vi) opt. forming a silicide cpd. layer o- the **polysilicon**; and (vii) providing surface contacts to the buried layers, **emitters**, **base** contacting **regions**, **MOS** gates, source and drain regions.

USE/ADVANTAGE - Provides bipolar and **CMOS** transitors on a single semiconductor substrate. Provides high peformance without high power consumption.

Dwg.3-5/19

Abstract (Equivalent): US 5541120 A

A method for forming an integrated circuit structure including complementary **PNP** and **NPN bipolar transistors** of similar profile and approximately matched performance and at least one field effect (**MOS**) transistor adjacent the bipolar transistors on a common substrate, comprising the steps of: defining at least one buried layer within the substrate; for each bipolar transistor, forming a bipolar transistor **intrinsic base region** within the substrate having a doping concentration different from that of the substrate; depositing only a single layer of **polysilicon** on the substrate; for each bipolar transistor, forming an insulating ring within the **polysilicon** layer around a

region where a bipolar transistor emitter is formed, the insulating ring having an inside region and an outside region of **polysilicon** ; for each bipolar transistor, selectively forming a self-aligned bipolar transistor emitter within the substrate below the inside regions of **polysilicon** layer; for each bipolar transistor, selectively forming an **extrinsic base** within the substrate below the outside region of **polysilicon** layer; where the emitters and **extrinsic bases** of the **NPN** and **PNP** **transistors** are formed in two drive-in steps; where an **N-type emitter** of the **NPN transistor** is formed simultaneously with an **N-type extrinsic base** of the **PNP transistor**; and where a **P-type** **emitter** of the **PNP transistor** is formed simultaneously with a **P-type extrinsic base** of the **NPN transistor**; for each **MOS** transistor, forming a **MOS** transistor gate from the single layer of **polysilicon**; for each **MOS** transistor, forming **MOS** transistor source and drain regions within the substrate; and providing surface contacts to the bipolar transistor **emitters** and **base** contacting **regions** and to the **MOS** transistor gate, source and drain regions.

US 5444285 A

IC structure includes complementary **PNP** and **NPN** **bipolar transistors** of similar profile and approx. matched performance and at least field effect **MOS** transistor adjacent the bipolar transistors on a common substrate. Emitters and extrinsic bars of the **NPN** and **PNP transistors** are formed in two drive in steps. An **n-type emitter** of the **NPN** **transistor** is formed simultaneously with an **n-type** **extrinsic base** of the NPP transistor. A **p-type** **emitter** of the **PNP transistor** is formed simultaneously with a **p-type** extrusion base of the **NPN transistor**. For each **MOS** transistor, a **MOS** transistor gate is formed within the single layer of the **polysilicon**. For each **MOS** transistor source and drain regions are formed within the substrate. Surface contacts to the bipolar transistor emitters and to the **MOS** transistors gate source and drain regions are provided.

ADVANTAGE - **High performance** device is provided with size constraints at a min.. Contact regions may be made of top surface.

Dwg.17/19

US 5409845 A

Complementary bipolar and **CMOS** semiconductor device is mfd. by a method in which devices are formed on a substrate and a single layer of poly-**Si** is formed on the structure. A photoresist mask is used to define and etch narrow ring slots (58) around each prospective emitter area in the poly-**Si** layer, which are filled with dielectric. Self-aligned emitters are formed below and inside the rings (64) and **base** contacting **regions** (68A, 68B) are formed outside. **MOS** gates, source and drain regions (78, 80) are formed and contacts are provided.

USE/ADVANTAGE - Good low current performance, relatively small **extrinsic bases** and emitters.

12,13/19

31/3,AB/13 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009541589
WPI Acc No: 1993-235132/199329
Related WPI Acc No: 1991-179660; 1992-317865; 1992-317866; 1992-407350; 1994-216945; 1994-233783
XRAM Acc No: C93-104825
XRPX Acc No: N93-180491
Cubic boron nitride bipolar transistor - formed using pulsed laser evaporation method and appropriately doped boron nitride target
Patent Assignee: GENERAL MOTORS CORP (GENK)
Inventor: DOLL G L; HENNEMAN L E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5227318	A	19930713	US 89446758	A	19891206	199329 B
			US 90523951	A	19900516	
			US 91703939	A	19910522	
			US 92829834	A	19920203	

Priority Applications (No Type Date): US 91703939 A 19910522; US 89446758 A 19891206; US 90523951 A 19900516; US 92829834 A 19920203
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5227318	A		10	H01L-021/265	Div ex application US 89446758
					CIP of application US 90523951
					Div ex application US 91703939
					Div ex patent US 5164810

Abstract (Basic): US 5227318 A

Forming a bipolar transistor suitable for use at high temps. comprises; 1) a **Si** substrate oriented along the (100) crystallographic plane, 400-700 deg. **C**; 2) providing a BN target in spaced relationship to the substrate; 3) laser ablating the BN target so as to evaporate material onto a surface of the substrate to form a first thin film layer of BN which is in epitaxial registry with the **Si** substrate. The thin film layer has a cubic crystallographic structure throughout, and appropriately doping the thin film layer to be an electroconductive **n-type** collector region; 4) laser ablating the BN target so as to evaporate material onto the collector region to form a second thin film layer of BN which is epitaxial w.r.t. the collector region, the second layer similarly having a cubic crystallographic structure throughout, and appropriately doping the second layer so as to form an electroconductive **p-type base region**; 5) laser ablating the BN target so as to evaporate material onto the **base region** to form a third thin film layer of BN, which is epitaxial w.r.t. the **base region**, the third layer similarly having a cubic crystallographic structure throughout, and appropriately doping the third layer so as to form an electroconductive **n-type** region; 6) forming electrical contacts onto the **Si** substrate, onto the **base region** and onto the **emitter region**, such that an **n-p-n bipolar transistor** is provided.

USE/ADVANTAGE - Bipolar transistor formed from epitaxial cubic BN suitable for use in **high** temp. and **high performance** applications. The transistors can be made smaller than conventional transistors.

(Dwg.0/2

31/3,AB/14 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009424322
WPI Acc No: 1993-117838/199314
XRAM Acc No: C93-052372
XRPX Acc No: N93-089797

Complementary bipolar transistors - formed on dielectrically isolated substrate giving high early voltage **high** frequency **performance** and **high** breakdown voltage

Patent Assignee: HARRIS CORP (HARO)
Inventor: BAJOR G; BEASOM J D; CRANDELL T L; DAVIS C K; JUNG T; RIVOLI A L

Number of Countries: 018 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9306622	A1	19930401	WO 92US8211	A	19920925	199314	B
EP 605634	A1	19940713	EP 92921300	A	19920925	199427	
			WO 92US8211	A	19920925		
JP 7502624	W	19950316	WO 92US8211	A	19920925	199519	
			JP 93506401	A	19920925		
US 5668397	A	19970916	US 91766201	A	19910927	199743	
			US 93131369	A	19931004		
US 5807780	A	19980915	US 91766201	A	19910927	199844	
			US 93131369	A	19931004		
			US 95462851	A	19950605		
US 5892264	A	19990406	US 93131369	A	19931004	199921	N
			US 97786569	A	19970121		
KR 292851	B	20010917	WO 92US8211	A	19920925	200231	
			KR 94700984	A	19940326		

Priority Applications (No Type Date): US 91766201 A 19910927; US 93131369 A 19931004; US 95462851 A 19950605; US 97786569 A 19970121
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9306622	A1	E	59	H01L-029/73	
Designated States (National): JP KR					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL SE					
EP 605634	A1	E		H01L-029/73	Based on patent WO 9306622
Designated States (Regional): DE FR GB IE IT NL					
JP 7502624	W		19	H01L-021/331	Based on patent WO 9306622
US 5668397	A		19	H01L-029/00	Cont of application US 91766201
US 5807780	A			H01L-021/331	Cont of application US 91766201 Div ex application US 93131369
US 5892264	A			H01L-029/00	Div ex application US 93131369 Div ex patent US 5668397
KR 292851	B			H01L-029/73	Previous Publ. patent KR 94702647

Abstract (Basic): WO 9306622 A

Bipolar transistor formed in an electrically isolated semiconductor island comprising; a) collector doped to a net first conductivity type and including a more heavily doped **region** b) **base** formed in a region doped to a net second conductivities type adjoining the collector **c**) emitter doped to a net first conductivity type adjoining the base. The transistor has an early voltage of at least 40 volts and a frequency response of at least 3GHz.

In an integrated circuit, a first **PNP transistor** is formed in a first electrically isolated semiconductor island and a second **NPN transistor** in a second island. The first transistor includes a **P** conductivity **type** collector having a heavily doped region adjoining a more lightly doped region of the

same type. The second transistor includes a **N**-conductivity **type** collector having a more heavily doped region of the same type.

Also claimed is the method of forming a pair of complementary bipolar transistors comprising the steps; a) forming a heavily doped **N-type** buried region in an electrically isolated semiconductor layer with **N-type** impurities. b) forming a heavily doped **P-type** buried region in a second electrically isolated semiconductor layer with **P-type** impurities having similar diffusion coefficient to the **N-type** such that when thermally processed the P and **N type** impurities diffuse similar distances within respective semiconductor layers.

ADVANTAGE - The method provides shallow emitters and small emitter to **extrinsic base** distance and **high performance**.

Dwg.2/12

Abstract (Equivalent): US 5668397 A

An integrated circuit along a semiconductor surface comprising at least one **NPN** and one **PNP** bipolar **transistors**, each of the transistors having a collector having a more heavily doped layer in it, a base and an emitter with a polycrystalline **silicon** contact, where: (a) the thickness of each base and the contiguous emitter and the doping profiles of it cooperating to provide an Early Voltage of Ea for each of the transistors, (i) the barrier provided by the polycrystalline **silicon** emitter contact and (ii) the thickness and doping profile of the emitter and the contiguous base cooperating to provide an emitter injection efficiency sufficient to produce a current gain of beta for each of the transistors, the product of Ea and beta for each of the transistors being not less than about 800 volts; (b) (i) the doping profile of the collector in the region immediately adjacent the base and (ii) the thickness and doping profile of the base cooperating to provide a collector-to-emitter breakdown voltage of not less than about 12 volts for each of the transistors; and (**c**) (i) the thickness of the base and the doping profile of it, (ii) the geometry and doping profile of the base underlying the contiguous emitter and (iii) the resistance of the base between the contiguous emitter and the contiguous polycrystalline **silicon** base contact cooperating to provide for each of the transistors a Ft of not less than about 3 GHz.

Dwg.9/21

31/3,AB/15 (Item 10 from file: 350)

DIALOG(R)File 350:Derwent WPIX

009190348

WPI Acc No: 1992-317784/199239

XRAM Acc No: C92-141138

XRPX Acc No: N92-243240

Heterojunction bipolar transistor without MISFIT dislocation - has **silicon@-germanium@** alloy and small atom insertion, and **high**-speed **performance**

Patent Assignee: HITACHI LTD (HITA)

Inventor: FUKAMI A; NAGANO T; SHOJI K

Number of Countries: 006 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 504875	A2	19920923	EP 92104781	A	19920319	199239	B
CA 2063220	A	19920921	CA 2063220	A	19920317	199250	

JP 5144834	A	19930611	JP 9157090	A	19910320	199328
US 5323031	A	19940621	US 92853819	A	19920319	199424
EP 504875	A3	19940518	EP 92104781	A	19920319	199524

Priority Applications (No Type Date): JP 9157090 A 19910320
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 504875	A2	E	30	H01L-029/73	
Designated States (Regional): DE FR GB					
JP 5144834	A		16	H01L-021/331	
US 5323031	A		26	H01L-031/072	
CA 2063220	A			H01L-021/331	
EP 504875	A3			H01L-029/73	

Abstract (Basic): EP 504875 A

A bipolar transistor, in which the effects of misfit dislocation at the heterojunction are minimised, includes a collector **region** (13), **base region** (12) of opposite conductivity type with a junction between them, **emitter region** (11) doped as the collector and with an emitter-base junction, and with the band gap of the emitter and base near the base-emitter junction narrowing from emitter to base near the base-emitter junction.

Also claimed is a transistor as above where collector, base, and emitter are of **Si** and **Ge** is mixed in the **emitter** and **base regions** near their junction, with its concn. increasing from emitter to base. Further claimed is a transistor as in the first claim above in which the **emitter** and **base regions** are of **Si-Ge** alloy and **Ge** concn. increases from emitter to base.

USE/ADVANTAGE - Bipolar transistors and methods of mfr. (claimed) are provided which are useful for HBTs for **BiCMOS**, logic gates, memory cells, and microprocessors. The effects of misfit dislocations at the heterojunction are minimised, **high**-speed **performance** is improved and leakage currents reduced.

Dwg.1A/19

Abstract (Equivalent): US 5323031 A

A bipolar transistor includes a collector region of a first conductivity type, opposite to the first conductivity type, which forms a collector-base junction at an interface between the **base region** and the collector **region**; and an **emitter region** of the first conductivity type which forms a base-emitter junction at an interface between the **emitter region** and the base **region**. Portions of the emitter **region** and the **base region** in proximity of the base-emitter junction are formed of **Si-Ge** alloy. The concn. of the **Ge** component of the **Si-Ge** alloy in each of the portions is increasing along a direction from the **emitter region** to the **base region**.

USE/ADVANTAGE - The bipolar transistor minimises the influences of the misfit dislocations which occur when the hetero-junction is formed.

Dwg.1a/19

31/3,AB/16 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008808006
WPI Acc No: 1991-312018/199143
XRAM Acc No: C91-135095

XRPX Acc No: N91-239147

Gate insulation region formation for field effect gate device - comprises forming on substrate, insulator region, partially masked poly-**silicon** layer and etched conductive region

Patent Assignee: NAT SEMICONDUCTOR CORP (NASC)
Inventor: BISWAL M; BLAIR C S; ILDEREM V; IRANMANESH A A; JEROME R C; RAJEEVA L; SOLHEIM A G; LAHRI R

Number of Countries: 007 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 452720	A	19911023	EP 91104940	A	19910328	199143 B
JP 4226066	A	19920814	JP 91144278	A	19910402	199239
US 5338694	A	19940816	US 90502943	A	19900402	199432
			US 92847876	A	19920309	
US 5338696	A	19940816	US 90502943	A	19900402	199432
			US 92847876	A	19920309	
			US 9322708	A	19930301	
EP 452720	A3	19941026	EP 91104940	A	19910328	199534
US 5661046	A	19970826	US 90502943	A	19900402	199740
			US 92847876	A	19920309	
			US 94285839	A	19940804	
KR 223098	B1	19991015	KR 914975	A	19910329	200108

Priority Applications (No Type Date): US 90502943 A 19900402; US 92847876 A 19920309; US 9322708 A 19930301; US 94285839 A 19940804

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 452720	A				
Designated States (Regional): DE FR GB IT					
JP 4226066	A		17	H01L-027/092	
US 5338694	A		15	H01L-021/265	Cont of application US 90502943
US 5338696	A		17	H01L-021/265	Cont of application US 90502943 Div ex application US 92847876
US 5661046	A			H01L-021/265	Cont of application US 90502943 Div ex application US 92847876 Div ex patent US 5338694
KR 223098	B1			H01L-027/10	

Abstract (Basic): EP 452720 A

A method of forming a gate insulating region for a field effect gate comprise forming: a) insulator region on semiconductor substate surface; b) first **polysilicon** layer on insulator; **c**) mask on portions of **polysilicon** layer, which define gate regions; d) **polysilicon** and insulator from unprotected regions of mask; e) conductive region along surface; and f) etching conductive region to form gate.

Method for fabricating field effect device of selected threshold voltage, contg. channel regions of first and second conductivity type, comprising: a) in substrate contg. surface of first and second regions, implant using first dopant in first region and second dopant into both regions; b) forming gate oxide regions on both regions and **c**) forming conductive gates on gate oxide regions.

USE/ADVANTAGE - Semiconductor devices can be made with improved performance, reduced size, and of simpler fabrication. Devices can be used with **high performance** Emitter Coupled Logic (ECL) standard cell designs, multiport 6 transistor memory cell, gate array designs with embedded memory etc. It has improved gate oxide formation and adjusting of the threshold voltage whilst also providing method of forming a **base region** in bipolar devices as a channel region in field effect devices in a BiCMO5 process. (23pp Dwg.No.1/27)

Abstract (Equivalent): US 5661046 A

A method of fabricating **BiCMOS** devices on a substrate with a selected threshold voltage for field effect devices, a first portion of said **BiCMOS** devices including said field effect devices having a channel region of a first conductivity type, a second portion of said **BiCMOS** devices including said field effect devices having a channel region of a second conductivity type, a third portion of said **BiCMOS** devices including a bipolar region, the method comprising the steps of:

a) in the substrate having a surface with first and second regions being adjacent to said bipolar region, implanting a first dopant in said first region, said first dopant of said first conductivity type;

b) implanting said first and said second regions with a second dopant, said second dopant of said second conductivity type, said first region having a net dopant concentration of said first conductivity type;

c) forming gate oxide regions on said first and said second regions; and

d) forming conductive gates on said gate oxide regions, said first region comprising said channel region of said first conductivity type, said second regions comprising said channel regions of said second conductivity type;

and wherein the step of implanting said first dopant in said first region is preceded by the step of providing a well region having the second conductivity dopant below said second regions, the threshold voltage of said field effect devices formed in said second regions is set by up-diffusing dopant from said well region in combination with said implant of said second dopant.

US 5338696 A

The semiconductor structure is formed by (a) masking regions including at least **base regions** of bipolar transistors, (b) implanting with a 1st type dopant to provide channel regions with 1st characteristics, (**c**) forming a poly-**Si** layer over at least the **base regions**, (d) masking regions including at least the channel regions of **FETs**, (e) implanting the poly-**Si** layer with a 1st-type dopant, and (f) diffusing dopants from the poly-**Si** layer into underlying **Si** to provide at least a portion of the **base regions** of the bipolar transistors with 2nd characteristics. The 1st and 2nd characteristics are dopant concns. or implant depths. The 1st dopant is implanted at 30-100 KeV and the 2nd dopant at 30-50 KeV.

USE/ADVANTAGE - Used to form **BiCMOS** devices. The devices have improved performance, reduced size and can be fabricated more simply and economically.

Dwg.1/5

US 5338694 A

Semiconductor devices are mfd. by (a) implanting **n-type** deposits to form an **n-type** buried layer in a **p-type** substrate, for **PMOS** and bipolar transistors, (b) forming a **p-type** buried layer for an **NMOS**-transistor and **p-type** channel stops adjacent a 1st region, (**c**) forming an **n-type** epitaxial **Si** layer, (d) forming field oxide regions adjacent the 1st, 2nd and 3rd regions, as well as between a sink and a **base region** of the 1st region, (e) implanting **n-type** dopants into the sink region to a 1st concn., (f) implanting **p-type** dopants into the 3rd region to a 2nd concn., (g) implanting **p-type** dopants into the 2nd and 3rd regions to adjust the threshold voltages of the **NMOS** and **PMOS** transistors, (h) forming an insulator region comprising a gate oxide layer, (i) forming a 1st poly-**Si** layer, (j) forming a

mask to define gate regions of **FETs**, (k) removing the poly-**Si** and insulator from unprotected regions, (l) forming a conductive region above the insulator comprising a 2nd poly-**Si** layer; (m) etching the conductive region to form the gates above the insulator regions, by masking and implanting **n-type** and **p-type** dopants into the 2nd poly-**Si** layer, and forming emitter, base and collector contacts for the bipolar transistors, and source and drain contacts for the **NMOS** and **PMOS** transistors, then (n) implanting **n-type** dopant into the **NMOS** to form a lightly doped diffusion, (o) implanting B in the **PMOS**, (p) forming sidewall oxide on all the transistor contacts, (q) removing sidewall oxide from exposed regions, (r) **p-type** doping of 1st and 3rd regions, (s) **n-type** doping of 2nd regions, (t) forming a refractory metal layer across the 1st, 2nd and 3rd regions and heating to form metal silicide where it meets **Si**, (u) removing unreacted metal, and (v) forming an interconnect system between the transistors.

ADVANTAGE - Improved performance, reduced size and more simple fabrication.

Dwg.2v/4

31/3,AB/17 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008793296
WPI Acc No: 1991-297310/199141
XRAM Acc No: C91-128526
XRPX Acc No: N91-227819

High performance semiconductor devices mfr. - by forming 1st protective region over active and exposing regions, etching, forming dielectric region on substrate, and then oxidising, etc

Patent Assignee: NAT SEMICONDUCTOR CORP (NASC)
Inventor: BASTAMI B; BISWAL M; BLAIR C S; BOUKNIGHT J L; DAVIES T; DELONG B ; GANSCHOW G E; ILDEREM V; IRANMANESH A; JEROME R C; LAHRI R; LEIBIGER S M; SOLHEIM A G; BASTANI B; IRANMANESH A A
Number of Countries: 006 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 450500	A	19911009	EP 91103938	A	19910328	199141	B
US 5139961	A	19920818	US 90503498	A	19900402	199236	
US 5242854	A	19930907	US 90503498	A	19900402	199337	
			US 92879650	A	19920507		
JP 6342802	A	19941213	JP 91144277	A	19910402	199509	
EP 450500	A3	19940518	EP 91104938	A	19910328	199524	
EP 450500	B1	19980513	EP 91104938	A	19910328	199823	
DE 69129379	E	19980618	DE 629379	A	19910328	199830	
			EP 91104938	A	19910328		

Priority Applications (No Type Date): US 90503498 A 19900402; US 92879650 A 19920507
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 450500	A		21		
Designated States (Regional): DE FR GB IT					
US 5139961	A		17	H01L-021/33	
US 5242854	A		16	H01L-021/302	Div ex application US 90503498
					Div ex patent US 5139961
JP 6342802	A		13	H01L-021/331	

EP 450500 B1 E 19 H01L-021/76
Designated States (Regional): DE FR GB IT
DE 69129379 E H01L-021/76 Based on patent EP 450500

Abstract (Basic): JP 6342802 A

Forming an isolation oxide region adjacent active regions in a semiconductor substrate having a first surface, comprising steps: (i) forming a first protective region over active regions and exposing first regions; (ii) etching substrate in first regions to form recess having horizontal regions, (iii) forming dielectric region on substrate, (iv) etching dielectric region to substantially remove from horizontal but not sidewall regions, (v) oxidising horizontal regions to form isolation oxide region in substrate.

Also, forming a **base region** for a bipolar transistor comprising: (i) providing a single crystal region of first conductivity type on substrate, (ii) forming a polycrystalline layer second conductivity type doped on single crystal region, (iii) diffusing dopant of second type into single crystal **region** to form **base region**.

USE/ADVANTAGE - Use for **high performance** semiconductor devices and advantageous over prior art in that device size can be reduced due to improved properties and methods of mfr. (21pp Dwg.No.1b/3)

EP 450500 A

Forming an isolation oxide region adjacent active regions in a semiconductor substrate having a first surface, comprising steps: (i) forming a first protective region over active regions and exposing first regions; (ii) etching substrate in first regions to form recess having horizontal regions, (iii) forming dielectric region on substrate, (iv) etching dielectric region to substantially remove from horizontal but not sidewall regions, (v) oxidising horizontal regions to form isolation oxide region in substrate.

Also, forming a **base region** for a bipolar transistor comprising: (i) providing a single crystal region of first conductivity type on substrate, (ii) forming a polycrystalline layer second conductivity type doped on single crystal region, (iii) diffusing dopant of second type into single crystal **region** to form **base region**.

USE/ADVANTAGE - Use for **high performance** semiconductor devices and advantageous over prior art in that device size can be reduced due to improved properties and methods of mfr. (21pp Dwg.No.1b/3)

Abstract (Equivalent): US 5242854 A

Formation comprises implanting a first conductivity buried layer in the active region and implanting a channel stop region of second conductivity in the substrate prior to forming an overlying epitaxial **Si** layer; forming a protective region over the buried layer and exposing first regions through which the epitaxial **Si** is etched to form recessed regions; forming a dielectric on the substrate and etching to leave the dielectric only on sidewalls; and oxidising horizontal regions to form the isolation oxide regions.

USE/ADVANTAGE - Used in semiconductor device mfr. Base resistance is reduced and the **polysilicon** to single-crystal contact resistance is eliminated.

Dwg.2c/3

US 5139961 A

The **base region** is formed by (a) providing a single crystal region of 1st conductivity type on a substrate, (b) forming a polycrystalline region on (a), at least portions of (b) being doped with a 2nd type dopant, (c) diffusing the dopant into the single

crystal region to form the **base region**, (d) implanting an **emitter** contact **region** at (b) with 1st type dopants, and (e) etching the (b) **region** to form the **emitter** contact. The single crystal region is epitaxial **Si** and the polycrystalline region is poly-**Si**. The junction depth of the transistor is less than 0.25 microns. A low resistance region is formed in the base and aligned with the emitter.

ADVANTAGE - Improved mfg. method allows improved devices to be produced e.g. with increased reliability, reduced base-collector capacitance, etc

Dwg.0/3

31/3,AB/18 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008432830
WPI Acc No: 1990-319830/199042
XRAM Acc No: C90-138442
XRPX Acc No: N90-245134

Bipolar complementary **MOS** device - compatible with standard semiconductor processing, with **FET** in first region with channel under insulated gate etc.

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: LECHATON J S; SCHEPIS D J
Number of Countries: 007 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4960726	A	19901002	US 89424363	A	19891019	199042	B
EP 424298	A	19910424	EP 90480128	A	19900829	199117	
CA 2024640	A	19910430				199128	
JP 3145759	A	19910620	JP 90224569	A	19900828	199131	
CA 2024640	C	19930727	CA 2024640	A	19900905	199336	
EP 424298	B1	19960410	EP 90480128	A	19900829	199619	
DE 69026460	E	19960515	DE 626460	A	19900829	199625	
			EP 90480128	A	19900829		

Priority Applications (No Type Date): US 89424363 A 19891019
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 424298	A				
Designated States (Regional): DE FR GB IT					
EP 424298	B1	E	10	H01L-021/82	
Designated States (Regional): DE FR GB IT					
DE 69026460	E			H01L-021/82	Based on patent EP 424298
CA 2024640	C			H01L-021/331	

Abstract (Basic): US 4960726 A

A method of providing a **BiCMOS**, having **high performance** in both bipolar and **FETs**, comprises providing a semiconductor substrate (22) with at least two electrically isolated device regions (40, 42, 44), forming and patterning an insulating layer (50) to expose part of the second device region, forming a layer of conductor (58) over the device regions which contacts the second region, and forming an aperture (68) in this layer over the second region. Parts of the second layer are removed to leave a base contact in the second device and a separate gate contact insulated from the frist device region, an **FET** (42, 44) is formed having a channel underlying the gate contact in the first region, and a **vertical** bipolar **transistor** formed having a **base region**

contacting the **base** contact in the second region (40).

Also claimed is a method as above in which an **intrinsic base region** is formed in the second device region through and after forming the aperture, parts of the conductive layer are removed to leave a base contact in the surface of the second device region and a separate gate contact as above, forming an **extrinsic base region**, and then forming the **FET** and bipolar transistor as above.

USE/ADVANTAGE - A method of fabricating a **BiCMOS** which yields **high performance** in both bipolar transistors and **FETs** is provided. The method is compatible with standard semiconductor mfg. methods and is not unduly complex. (9pp Dwg.No 10/10)

Abstract (Equivalent): EP 424298 B

A method of forming **NPN bipolar** and CMOSFET devices in a **P type** semiconductor substrate (22) provided with an overlying N+ buried layer (24) and a top epitaxial layer (26) formed thereon to form a structure which includes at least first (40), second (42) and third electrically isolated device regions, the conductivity of the epitaxial layer in the said second region having been converted to **P type** and in said first and third regions to **N type**, said method comprising the steps of: a) forming a first layer (50,52) onto the structure which consists of a thin dielectric layer (50) to be used as the gate dielectric of the **CMOS FETs**, covered by a **polysilicon** layer (52); b) patterning said first layer to expose the epitaxial layer at the first device region location; **c**) forming a second layer of a **polysilicon** material (58) onto the structure which is doped with **P type** dopant above the said first and third device regions and with **N type** dopant above said second device region; d) forming a third layer (62,64) of insulating material over said second layer; e) forming an aperture (68) in said second and third layers at the location where the **intrinsic base** is to be formed in said first device region; f) forming the **intrinsic base** (69) of the **NPN bipolar transistor**; g) forming insulating sidewalls (70) on the exposed walls of the second layer of **polysilicon**; h) depositing a fourth layer (72) of N+ **polysilicon** that in particular fills the said opening and comes into contact with said **intrinsic base**; i) removing said fourth layer except at the location of said opening to form a raised contact; j) patterning said second and third layers above second and third device regions, so that the gate electrodes of the NFET (58A) and PFET (58C) are formed; k) forming the **extrinsic base** (80) and the emitter (82) of the **NPN transistor** by out diffusing the dopant contained in said second and fourth layers of polycrystalline **silicon** into said first device region; l) terminating the structure using conventional processing steps to form the source and drains of the **FETs** and contacts of all the devices.

(Dwg.2/10

31/3,AB/19 (Item 14 from file: 350)

DIALOG(R)File 350:Derwent WPIX

007861735

WPI Acc No: 1989-126847/198917

XRAM Acc No: C89-104206

XRPX Acc No: N89-178514

Bipolar semiconductor device integrated circuit prepn. - by forming thin film rugged surface by radio frequency bias sputtering Dwg 1/2

Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 1073766	A	19890320	JP 87229746	A	19870916	198917	B
GB 2209872	A	19890524	GB 8821635	A	19880915	198921	
US 4866000	A	19890912				198946	
GB 2209872	B	19910522				199121	

Priority Applications (No Type Date): JP 87229746 A 19870916
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 1073766	A		26		

Abstract (Basic): JP 1073766 A

Semiconductor integrated circuits mfr. on semiconductor substrate having 1st type of conductivity comprises a) forming 1st film on surface of region which is to become an active region with 2nd type of conductivity on the substrate, b) implanting 1st dopant with 1st type of conductivity through 1st film, **c**) forming 2nd film on structure thus obtd., d) selectively removing regions of 1st and 2nd films in a region which will become a **base** electrode **region** , e) forming 3rd film of polycrystalline **Si** on above structure, several concavities being gormed on corresp. regions of 3rd film, f) implanting 2nd dopant into 3rd film, g) diffusing the 2nd dopant from 3rd film into all or part of active region, h) forming 4th film by RF-bias sputtering in concavities formed in preceding step, at central part between concavitied anda t region where a collector electrode will be formed (this central part is positioned directly over a **region** where an **emitter** will be , formed), i) removing 4th film which has been formed outside active region, leaving 4th film over the emitter, base electrode and collectro electrode contact regions, j) selectively removing the parts of 3rd film that are above 2nd film and not covered by 4th film, k) removing 4th film completely, l) forming 5th film by RF-bias sputtering, m) forming windows and exposing emitter and collector electrode contact regions by selectively removing parts of 1st, 2nd and 3rd film, n) forming 6th film, and doping this to give 2nd type of conductivity, o) selectively removing the portion of 6th film which is above 2nd film, and p) diffusing dopant from 6th film into active region.

USE/ADVANTAGE - The method of mfg. bipolar semiconductor integrated circuits, which prior art limitations imposed on switching speed of transistor by the existence of a heavily-doped base layer. (First major country equivalent J01073766-A)

Dwg.2/9

GB 2209872 B

Semiconductor integrated circuits mfr. on semiconductor substrate having 1st type of conductivity comprises a) forming 1st film on surface of region which is to become an active region with 2nd type of conductivity on the substrate, b) implanting 1st dopant with 1st type of conductivity through 1st film, **c**) forming 2nd film on structure thus obtd., d) selectively removing regions of 1st and 2nd films in a region which will become a **base** electrode **region** , e) forming 3rd film of polycrystalline **Si** on above structure, several concavities being gormed on corresp. regions of 3rd film, f) implanting 2nd dopant into 3rd film, g) diffusing the 2nd dopant from 3rd film into all or part of active region, h) forming 4th film by RF-bias sputtering in concavities formed in preceding step, at central part between concavitied anda t region where a collector electrode will be formed (this central part is positioned directly over a **region**

where an **emitter** will be , formed), i) removing 4th film which has been formed outside active region, leaving 4th film over the emitter, base electrode and collectro electrode contact regions, j) selectively removing the parts of 3rd film that are above 2nd film and not covered by 4th film, k) removing 4th film completely, l) forming 5th film by RF-bias sputtering, m) forming windows and exposing emitter and collector electrode contact regions by selectively removing parts of 1st, 2nd and 3rd film, n) forming 6th film, and doping this to give 2nd type of conductivity, o) selectively removing the portion of 6th film which is above 2nd film, and p) diffusing dopant from 6th film into active region.

USE/ADVANTAGE - The method of mfg. bipolar semiconductor integrated circuits, which prior art limitations imposed on switching speed of transistor by the existence of a heavily-doped base layer. (First major country equivalent J01073766-A) (26pp Dwg.No.2/9

Abstract (Equivalent): GB 2209872 B

A method of fabrication of semiconductor integrated circuits on a semiconductor substrate having a first type of conductivity, comprising the steps of: (a) forming a first film (105) on the surface of a region which is to become an active region having a second type of conductivity on said semiconductor substrate: (b) implanting a first dopant having the first type of conductivity through said first film (105) in part of the surface region of said active region; (**c**) forming a second film (107) on the surfaces of the structure obtained by the preceding steps; (d) selectively removing regions (108) of said second film (107) and said first film (105) on a region which is to become a **base** electrode **region** (119); (e) forming a third film (109) of polycrystalline **silicon** on the surface of the structure obtained by the preceding steps; a plurality of concavities being formed on the regions (108) or said third film (109); (f) implanting a second dopant into said third film (109); (g) diffusing said second dopant from said third film (109) into part of all of said active region; (h) forming a fourth film (112) by an RF-bias sputtering in the concavities formed in the preceding step (e) at the central part between said concavities and at a region where a collector electrode contact will be formed, said central part being positioned directly over a **region** where an **emitter** will be formed (118), said fourth film (112) being also formed outside of said active region; (i) removing said fourth film (112) formed outside of said active region to leave said fourth film (112) over the **emitter region** (118), the **base** electrode **region** (119) and the collector electrode contact region (121); (j) selectively removing those parts of said third film (109) that are disposed above the surface of said second film (107) and are not covered by said fourth film (112); (k) completely removing said fourth film (112) to leave convexes (109-1, 109-2) over the **emitter region** (118) and at the collector el

Abstract (Equivalent): US 4866000 A

Semiconductor integrated circuits are fabricated on a semiconductor substrate having a first type of conductivity, by firstly forming a first film implanted with a first dopant, having the first type of conductivity. A second film (107) is formed on the surfaces of the structure obtd by the preceding steps. A third film (109) is formed of polycrystalline **silicon** on the surface of the structure obtd by the preceding steps, a number of concavities being formed on the regions (108) of film (109). A second dopant is implanted into film (109), then diffused from film (109), into part or all of the active region. A fourth film (112) is formed by an RF-bias sputtering in the concavities formed in the relevant preceding step, at the central part between the concavities, at a region where a collector electrode

contact will be formed, and also outside the active region. Film (112) formed outside the active region is removed, to leave film (112) over an **emitter region** (118), the **base** electrode **region** (119) and the collector electrode contact region (121). A fifth film is formed by an RF-bias sputtering on the structure obtd by the preceding steps, the surface of the resultant fifth film (114) being coplanar with the surface of film (109). A sixth film (117) is formed on the surface of the active region. A third dopant is doped into film (117), the third dopant having a second type of conductivity. That portion of film (117) disposed above the surface of film (107) is selectively removed. Finally, the third dopant is diffused from film (117) into the active region.

ADVANTAGE - Small, **high** speed, **high performance** transistors, can be made easily and with high reproducibility. (17pp)

31/3,AB/20 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007735997
WPI Acc No: 1989-001109/198901
XRAM Acc No: C89-000425
XRPX Acc No: N89-000897

Mfg. **MOS** and bipolar transistors on common substrate - involves implanting impurity ions in channel formation region with interposed dummy gate insulation film

Patent Assignee: TOSHIBA KK (TOKE)
Inventor: MAEDA T; MAKITA K
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 296627	A	19881228	EP 88110143	A	19880624	198901	B
JP 64002347	A	19890106	JP 87156443	A	19870625	198907	
JP 1059849	A	19890307	JP 87216666	A	19870831	198915	
US 4931407	A	19900605	US 88211010	A	19880624	199026	
JP 91051310	B	19910806	JP 87216666	A	19870831	199135	

Priority Applications (No Type Date): JP 87216666 A 19870831; JP 87156443 A 19870625
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 296627	A	E	12		

Designated States (Regional): DE FR GB

Abstract (Basic): EP 296627 A

Method for mfg. a semiconductor device comprises implanting impurity ions into a channel formation region of a **MOS** transistor, when forming bipolar and **MOS** transistors on the same substrate (14) with a dummy gate insulating film interposed, and implanting impurity ions to give an internal **base** formation **region** (34) of the bipolar transistor subsequent to forming a gate insulating film (23).

Also claimed is a method of mfg. a semiconductor device which comprises implanting ions to allow control of **MOS** transistor threshold levels, forming a gate electrode (24) over the transistor, then source and drain regions (26, 32) using the electrode (24) as a mask. Bipolar transistor external (27) and internal (34) **base** **regions** in contact are then formed by ion implantation, and a complete insulating interlayer (24) is deposited, followed by making an

opening to the internal base (34). A poly-**Si** layer is deposited and an **emitter region** and electrode formed by implantation into the internal base (34) with the poly-**Si** layer interposed.

USE/ADVANTAGE - The method gives **high performance** bipolar transistors on a common substrate with **MOS** devices. Transistors with increased current amplification factors (200) and cut-off frequency (10GHz), and lower emitter resistance (30 ohms) are made at the same time as **CMOS** transistors.

Abstract (Equivalent): US 4931407 A

Mfr. of a semiconductor device comprises (a) implanting impurity ions into a channel formation region to form a **MOS** transistor with a dummy gate insulating film, and (b) implanting impurity ions into an internal **base** formation **region** to form a bipolar subsequent to forming a gate insulating film. An emitter electrode of the bipolar transistor is formed by firstly depositing 500 - 2000 Angstrom layer of poly-**Si** on the gate gate during step (b); opening an emitter contact hole by etching the poly-**Si** layer and the gate insulating film; then depositing a second poly-**Si** layer of 100-1000 Angstrom on the surface of the resultant semiconductor substrate. The resultant semiconductor is subjected to a heat treatment, 10-60 sec. at 950-1100 deg.**C**, to reduce the emitter resistance.

USE/ADVANTAGE - Semiconductor devices with **MOS** transistors and **high performance** bipolar transistors can be mfr. on a common substrate. (6pp)

31/3,AB/21 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007690769
WPI Acc No: 1988-324701/198846
XRAM Acc No: C88-143266
XRPX Acc No: N88-246037
Vertical bipolar **transistor** - comprises **N-type emitter** on substrate in contact with self-aligned sidewall, **P-type extrinsic base** and **intrinsic base**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: MONKOWSKI M D; SHEPARD J F
Number of Countries: 014 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 290763	A	19881117	EP 88104842	A	19880325	198846 B
BR 8801815	A	19881129				198902
JP 63292674	A	19881129	JP 8887422	A	19880411	198902
AU 8815667	A	19881117				198911
US 4847670	A	19890711	US 8748346	A	19870511	198935
US 4916083	A	19900410	US 89318984	A	19890306	199020
CA 1277780	C	19901211				199104
EP 290763	B1	19931006	EP 88104842	A	19880325	199340
DE 3884665	G	19931111	DE 3884665	A	19880325	199346
			EP 88104842	A	19880325	

Priority Applications (No Type Date): US 8748346 A 19870511; US 89318984 A 19890306
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 290763	A	E	14		

Designated States (Regional): CH DE ES FR GB IT LI NL SE

US 4847670 A 10
EP 290763 B1 E 14 H01L-029/08
Designated States (Regional): CH DE ES FR GB IT LI NL SE
DE 3884665 G H01L-029/08 Based on patent EP 290763

Abstract (Basic): EP 290763 A

A **vertical** bipolar **transistor** comprises an **N-type emitter** (38) on a semiconductor substrate (10), the emitter being contacted by a self-aligned conductive sidewall (32) joined to a horizontal conductive link (20,46), a **P-type extrinsic base** (42) recessed below the emitter (38) and laterally sepd. from it by a vertical insulation sidewall, and a **P-type intrinsic base** (40) directly under the emitter and contiguous with the **extrinsic base** (42) which has the same vertical and lateral dimensions.

The conductive link is **N-type** polycide and also a conductive silicide layer lies above and self-aligned with the **extrinsic base** and is recessed below the emitter. The self-aligned sidewall (32) is of **N-type polysilicon** and the transistor further comprises a horizontal insulation layer between link and substrate which contacts the self-aligned sidewall. There is also an **N-type** collector (14) in the substrate. Also claimed is that the emitter is U-shaped in a perspective view and that the emitter is contacted on the top by **N-type** sidewall material which is contiguous and an **N-type** pad. Further claimed are processes for forming bipolar transistors as described.

USE/ADVANTAGE - Although there has been much progress in developing small, high-speed devices such as **polysilicon** self-aligned bipolar transistors, there is need for a device in which transistor action is confined to a very small area away from the device contact regions. This requires a small emitter to tight tolerances, minimal base-collector junction depth and low contact resistances. This meets these needs and provides three embodiments of a new **high-performance** transistor and processes for their mfr.

8/17

Abstract (Equivalent): EP 290763 B

A **vertical** bipolar **transistor** comprising a collector region (14) of a first conductivity **type** (**N**); a **base region** of a second type of conductivity (P) including an **intrinsic base region** (40,80,116) and an **extrinsic base region** (42,84,120) formed within said collector region and having a recess with respect to the collector region major surface substantially corresponding to the said **extrinsic base region**, said **intrinsic base** extending to said major surface adjacent to the recess; a first insulating layer (18,62,100) formed on said collector region having a substantially vertial wall to partly expose said **intrinsic base region** on said major surface; a first conductive layer (30,68,112) of said first conductivity **type** (**N**) forming at least a sidewall (32,74,112) on the exposed portion on said major surface of the **intrinsic base region** abutting said wall of the first insulating layer; a second insulating layer (36',82,118) formed on said conductive sidewall and on the adjacent wall of the recess; an **emitter region** of said first type of conductivity (N) of a width substantially that of said sidewall formed in said **intrinsic base region** and adjacent to said recess; a global passivating layer (48); a base contact (54) with said **extrinsic base region**; an **emitter** contact (52) with said **emitter region** via said conductive sidewall; and a collector contact (50) with said

collector region.
Dwg.1/17

Abstract (Equivalent): US 4916083 A

Vertical bipolar **transistor** is made by initially forming an insulator condcutor dual layer with a vertical surface on a substrate provided with an epitaxial layer. An **intrinsic base region** is formed in the epitaxial layer adjacent to the wall and doped material is provided or the epitaxial layer as a sidewall abutting the vertical surface. The epitaxial layer not masked by the sidewall and the dual layer below the surface of the remainder of the epitaxial layer are anisotropically etched. Dopant from the sidewall is diffused into the **intrinsic base** to form an emitter and an insulator is established on the sidewall. An **extrinsic base** is formed in the recessed epitaxial layer. ADVANTAGE - Lithography-independent and tightly controlled submicron wide emitter is obtd.
(11pp)

US 4847670 A

Bipolar transistor comprises (a) a first conductivity type semiconductor substrate a portion of which is recessed below a major surface of the substrate, the recessed portion having vertical walls, (b) a multilayer insulator-conductor-insulator formed on (a) with the multilayer having (1) an opening provided with vertical walls exposing a portion of (a) including the recessed portion, and (2) submicron-wide sidewall of first conductivity type material formed on the walls, (**c**) an emitter of submicron depth and of a width of that of the sidewall formed in (a), peripheral to the recessed portion directly underneath the sidewall which serves as self-aligned contact to (**c**), (d) an **extrinsic base** formed in the recessed portion, the **base region** having a conductive silicide contact recessed below the level of (**c**), the contact being isolated from (**c**) by an insulator formed on the walls of the recess, and (e) an **intrinsic base** formed in (a) lying directly underneath (**c**) and contiguous with (d). ADVANTAGE - New transistor is lithography-independent and of tightly controlled submicron width.
(10pp

31/3,AB/22 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007523068
WPI Acc No: 1988-157001/198823
XRAM Acc No: C88-069943
XRPX Acc No: N88-119979

Bipolar transistor - mfd. by transversely arranging collector, base and emitter layers in sequence through **monosilicon** layer formed on insulation layer

Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Inventor: KAZUYUKI S; KYUSAKU N; SIGERU K; TASUHIKO I
Number of Countries: 003 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2198285	A	19880608	GB 8725631	A	19871102	198823	B
JP 63140571	A	19880613	JP 86287325	A	19861201	198829	
GB 2198285	B	19900801				199031	
US 4990991	A	19910205	US 87115049	A	19871030	199108	
US 5070030	A	19911203	US 90606828	A	19901031	199151	

Priority Applications (No Type Date): JP 86287325 A 19861201
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
GB 2198285 A 32

Abstract (Basic): GB 2198285 A

High speed bipolar transistor comprises: a semiconductor substrate with an insulation layer; a layer of first type forming element regions; an insulation film for isolating adjacent mono-**Si** regions; first and second type diffusion layers (33,34) formed in the mono-**Si** layer by transverse diffusion in sequence from a hole defined in the mono-**Si** layer to reach the underlying insulation layer; and contacts to the mono-**Si** layer (35) and each diffusion layer (33,34).

Pref. the first and second diffusion **regions** are respectively **emitter** and **base regions** and the mono-**Si** region is a collector region.

ADVANTAGE - Structure reduces parasitic capacitance between base and collector and removes p-n junction capacitance between collector and substrate to achieve high speed operation.

2/5

Abstract (Equivalent): GB 2198285 B

A bipolar transistor comprising: a. a semi-conductor substrate at least a surface of which is insulating, b. a monocrystal **silicon** layer of a first conductivity type formed on the said surface, **c.** an insulating layer formed on the said substrate, the insulating layer defining an isolation region around said monocrystal **silicon** layer, d.

first and second diffusion layers formed by sequential transverse diffusion into a region of the monocrystal **silicon** layer surrounding a hole extending through the monocrystal **silicon** layer to the said surface, the first and second diffusion layers being formed such that the first diffusion layer is annular and extends around the second diffusion layer, the second diffusion layer is annular and positioned between the said hole and the first diffusion layer, the first diffusion layer is of the second conductivity type, and the second diffusion layer is of the first conductivity type and, e. electrodes connected to the monocrystal **silicon** layer the first diffusion layer and the second diffusion layer respectively via mutually isolated connecting layers.

Abstract (Equivalent): US 5070030 A

Mfg. bipolar transistor comprises (a) oxidising surface of semiconductor substrate to form monocrystal **silicon** layer; (b) forming isolation region for inter-element isolation on **silicon** layer other than element region; (**c**) introducing impurity close to isolation film, activating by heating; (d) forming insulation layer, depositing polycrystal **silicon** layer; (e) opening polycrystal **silicon** layer and insulating layer exposing surface of monocrystal; (f) depositing second polycrystal layer; (g) diffusing second impurity into polycrystal layers; (h) partially removing two polycrystal **silicon** layers; (i) patterning; (j) depositing nitride film over entire chip surface; (k) oxidising entire surface then removing nitride film; (l) depositing third polycrystal **silicon** layer; (m) coating insulating material over entire chip surface; (n) removing insulating material; (o) forming contact holes in insulation layer, on co

US 4990991 A

Bipolar transistor for achieving high-speed operation comprises (a) a semiconductor substrate having at least one surface part which is

finished as an insulation layer; (b) a first conductivity type monocrystal **silicon** layer formed on an element region of (a); (**c**) an insulation film for inter-element isolation, formed on an isolation region of (a) for isolating adjacent ones of layer (b); (d) a second conductivity type diffusion layer and a first conductivity type diffusion layer formed in layer (b), by transverse ' diffusion in sequence from a hole defined in a part of layer (b), to reach the insulation layer of (a); and (e) electrode extracting layers connected to layers (b), (d) and the first conductivity type diffusion layer, respectively, while being isolated from each other. ADVANTAGE - New transistor can further reduce parasitic capacity between a base and a collector, and that between a collector and a substrateg to attain **high**-speed **performance**. (14pp)

31/3,AB/23 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007382110
WPI Acc No: 1988-016045/198803
XRAM Acc No: C88-006997
XRPX Acc No: N88-011980
Simultaneous bipolar and **CMOS** fabrication - using minimal no. of masks giving good yield of **high performance** devices
Patent Assignee: FAIRCHILD SEMI COND (FAIR-N); FAIRCHILD SEMICONDUCTOR CORP (FAIH); NAT SEMICONDUCTOR CORP (NASC)
Inventor: MANOLIU J; TUNTASOOD P
Number of Countries: 008 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 253724	A	19880120	EP 87401631	A	19870710	198803 B
JP 63080560	A	19880411	JP 87176068	A	19870716	198820
US 5023193	A	19910611	US 88253946	A	19881003	199126
US 5407840	A	19950418	US 86887006	A	19860716	199521
			US 88253946	A	19881003	
			US 91697360	A	19910508	
			US 92925807	A	19920804	
KR 9512742	B1	19951020	KR 877684	A	19870716	199851

Priority Applications (No Type Date): US 86887006 A 19860716; US 88253946 A 19881003; US 91697360 A 19910508; US 92925807 A 19920804
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 253724	A	E	13		
Designated States (Regional): DE FR GB IT NL					
US 5023193	A		12		
US 5407840	A		14	H01L-021/328	Cont of application US 86887006
					Cont of application US 88253946
					Cont of application US 91697360
					Cont of patent US 5023193
KR 9512742	B1			H01L-027/06	

Abstract (Basic): EP 253724 A
A process for the simultaneous fabrication of bipolar and complementary field effect transistors uses as little as 6 masks prior to the contact mask. with the first mask two impurities of opposite type to the substrate (such as phosphorus and arsenic on O-type **silicon**) are implanted where buried layers are to be formed.An overall **P-type** cover and an undoped **silicon** epitaxial layer follow. Using the second mask this is N-doped (27,28) over the

buried layers. the structure is then heated to 1050-1100 deg.**C** in nitrogen for 1-2 hrs. to diffuse the P and N impurities used to form the buried layers and wells. With the third mask the required field oxide regions are defined.

Following the front-end process, the minimum mask back-end process begins with a fourth mask to define the bipolar transistor base by boron ion implantation. The fifth mask defines the gate electrodes of polycrystalline **Si** deposited by chemical vapour disposition and doped with phosphorus to improve its conductivity. The **NMOS** source and drain regions and the bipolar device emitter and collector are defined by the sixth mask using arsenic ion implantation. The structure is then annealed at 900 deg.**C**, oxidised and electrical connections made. An alternative back-end process employs more masks but gives **higher performance** transistors.

USE/ADVANTAGE - The desirable integration of bipolar-and **CMOS**-forming processes on a single wafer is currently complex and lengthly, with many masking steps and may lead to poor yields. The new process uses a minimal number of masking steps yet results in **high performance** devices. It allows **CMOS** devices with a 1 micron gate while providing high-speed switching bipolar devices.

Abstract (Equivalent): US 5407840 A

A semiconductor structure is fabricated by (a) depositing an epitaxial layer of semiconductor material over a semiconductor substrate, (b) implanting 1st conductivity type impurity into a bipolar region of the epitaxial layer to form a base of a bipolar transistor, (**c**) implanting 2nd-type impurity in the bipolar region of the epitaxial layer to form a collector contact and emitter of the bipolar transistor and into an **FET** region of the epitaxial layer to form source and drain regions of an **FET**, (d) masking a **base** contact **region** of the **base** of the bipolar transistor from the 2nd type implant, and (e) oxidising the epitaxial layer to form a differential thickness oxide layer which is thicker over the source and drain **regions**, collector contact and **emitter** than over the **base** contact **region**.

ADVANTAGE - **High performance** and **high** switching speeds. Minimum number of masking steps.

Dwg.6/14

US 5023193 A

The method comprises (a) blanket implanting a 1st type impurity into a semiconductor substrate (b) implanting a 2nd type impurity into a 1st region where a buried layer is to be formed (**c**) depositing an epitaxial layer (d) implanting a 2nd type impurity into (**c**), (e) heating to cause contact of both 2nd type impurities and form 1st and 2nd type wells, (f) deposting a nitride layer (g) etching to form openings (h) implanting an impurity into the epitaxial layer using the nitride portions of the epitaxial layer, (j) depositing layer using the nitride layer as a mask, (i) forming an oxide layer overlying the exposed portions of the epitaxial layer, (j) depositing an oxide-exclusion layer, (k) etching (j) to form openings, (l) implanting an impurity exposed parts of the epitaxial layer to form an opening to define a **base region**, (o) implanting 1st-type impurity into the **base region**, (p) removing the mask (q) blanket implanting 1st type impurity into the epitaxial layer (r) implanting 2nd type impurity into the exposed portions of the 1st type well where a source and drain are to be formed, (s) implanting 2nd-type well where a collector and emitter are to be formed, and (t) oxidising the exposed protions of the epitaxial layer to form a differential oxide layer which is thinner over the exposed portions which do not have implanted 2nd-type impurity than over the exposed portions which do contain impurity.

USE/ADVANTAGE - Used for mfg. a **BICMOS** in a semiconductor substrate. Only six masks are required, and the devices have good performance.

31/3,AB/24 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007275645
WPI Acc No: 1987-272652/198739
XRAM Acc No: C87-115749
XRPX Acc No: N87-204201
CMOS compatible bipolar transistor mfr. - using emitter as mask for **base** contact **region** alignment
Patent Assignee: NORTHERN TELECOM EUROPE LTD (NELE); NORTHERN TELECOM LTD (NELE); STC PLC (STTE)
Inventor: BAKER R L; BLOMLEY P F; SCOVELL P D
Number of Countries: 007 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 239216	A	19870930	EP 87301212	A	19870212	198739	B
GB 2188479	A	19870930	GB 86607594	A	19860326	198739	
JP 62235769	A	19871015	JP 8771296	A	19870325	198747	
GB 2188479	B	19900523				199021	
US 4965216	A	19901023	US 90471031	A	19900126	199045	
KR 9503931	B1	19950421	KR 872112	A	19870310	199710	

Priority Applications (No Type Date): GB 867594 A 19860326; GB 86607594 A 19860326
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 239216	A	E	8		
Designated States (Regional): BE GB IT NL					
KR 9503931	B1			H01L-029/72	

Abstract (Basic): EP 239216 A
(A) In bipolar transistor mfr. by forming a p- or **n-type** layer in a doped n- or **p- type** well of a semiconductor substrate, providing an emitter in contact with the layer, forming p(+)- or **n**(+)- **type base** contact **regions** extending through the layer, providing a collector contact region and applying contacts to the collector contact region and to the base and emitter, the novelty is that the emitter provides a mask for alignment of the **base** contact **regions**.
(B) Simultaneous mfr. of a bipolar transistor and a complementary pair of **MOSFETS**, each disposed in a respective well in a common substrate, involves (I) forming field oxide to define device regions; (ii) masking the substrate and forming a window in the mask to expose the entire bipolar device region; (iii) implanting dopant through the window to define a layer in the bipolar region; (iv) selectively depositing **polysilicon** to define the emitter of the bipolar transistors and the gates the of **MOSFETS**; (v) implanting source and drain regions of one **MOSFET** and **base** contact **regions** of the bipolar transistor using the **polysilicon** areas as implantation mask; (vi) implanting a collector contact for the bipolar transistor and source and drain regions of the other **MOSFET**; (vii) providing an insulating layer over the structure; and (viii) providing electrical contacts to the transistors.
(**C**) Also claimed is an IC comprising several transistors

mfd. by process (A).
Dwg.7/7
Abstract (Equivalent): GB 2188479 B
A method of fabricating a **polysilicon** emitter bipolar transistor, the method including providing an **n-type** well in a silicone semiconductor substrate, ion implanting a **p-type** layer in said well whereby to provide a **base region** for the transistor, providing a **polysilicon** emitter body over a portion of said **p-type** layer, ion implanting a **p(+)-type** dopant into the portion of the **p-type** layer unprotected by the emitter body whereby to provide **base** contact **regions** contiguous with the **p-type** layer, providing an **n(+)-type** collector contact region in said well, and providing a metallisation pattern whereby to contact the base contact and collector contact regions.f
Abstract (Equivalent): US 4965216 A
Poly-**Si** emitter bipolar transistor and complementary n-channel and p-channel field effect transistors are formed on a **p-type Si** substrate in which **n-type** wells are formed. Device areass are defined and a layer of **p-type** dopant is formed by implanting a window being formed in the oxide covering the layer. A layer of undoped poly-**Si** is deposited and implanted and patterned to produce emitter and gates. B is implanted to give base contact regims for the bipolar transistor, substrate contact for the n-channel **MOS** transistor and source and drain for the **p-type MOS** transistor. Through patterning, windows are defined for implantation of e. g. As for collector contact of the bipolar transistor, source and drain regas for the n-channel **MOS** transistor and well contact for the p-channel transistor. Wafer is oxidised and a layer of glass is deposited.
ADVANTAGE - Good yield and **high performance** of all transistors. (8pp)

31/3,AB/25 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004271216
WPI Acc No: 1985-098094/198516
XRAM Acc No: C85-042506
XRPX Acc No: N85-073503
CMOS and **vertical** bipolar **transistor** mfr. - uses low dose blanket implant to form base and selective implant to form emitter
Patent Assignee: NCR CORP (NATC)
Inventor: SULLIVAN P A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4507847	A	19850402	US 82391068	A	19820622	198516	B

Priority Applications (No Type Date): US 82391068 A 19820622
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4507847	A		12		

Abstract (Basic): US 4507847 A
The devices are formed in the same wafer by (a) forming n and **p type** regions in the wafer surface; (b) forming isolation oxide, defining locations of n-channel, p-channel and bipolar

transistors; (c) forming self-aligned **Si** gate n- and p-channel devices (ION, IOP) in the surface regions; (d) forming the bipolar transistor base (32) in a second conductivity type region by implanting a low blanket dose of first type ions, at a level less than 10% the dose used to form **MOS** source and drain regions (e) forming a dielectric layer (34) having openings to selected contact **regions**, including an **emitter** contact window over the **base region** delineating the **emitter region** (37) and contacts to **MOS** regions; (f) forming a 0.05-0.5 micron thick **Si** layer (36) on the dielectric and contact windows; (g) selectively implanting second type ions into the emitter contact and contacts to second type **regions**; (h) diffusing base and **emitter regions** to predetermined depths; (i) depositing a metal layer on the **Si**; (j) selectively patterning the dual **Si**-metal contact layer; and (k) forming a passivation layer on the device.

ADVANTAGE - Only one extra masking step (for g) is required over **CMOS** device mfr. to produce the **high performance** bipolar transistor, with no adverse effects on the **CMOS** devices. The **Si** layer of (f) improves reliability of the **CMOS** devices.

11/11

31/3,AB/26 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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003793872
WPI Acc No: 1983-790110/198342
XRAM Acc No: C83-100039
XRPX Acc No: N83-183768
Base and **emitter regions** of non bipolar transistor - prepd. by implanting dopants in **polysilicon** with double diffusion
Patent Assignee: IBM CORP (IBMC)
Inventor: BARSON F; KEMLAGE B M
Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 90940	A	19831012				198342	B
JP 58154267	A	19830913				198342	
US 4431460	A	19840214	US 82355633	A	19820308	198409	
EP 90940	B	19900523				199021	
DE 3381605	G	19900628				199027	
JP 91076575	B	19911205	JP 833621	A	19830114	199202	

Priority Applications (No Type Date): US 82355633 A 19820308
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 90940	A	E	29		
Designated States (Regional): DE FR GB					
EP 90940	B				
Designated States (Regional): DE FR GB					

Abstract (Basic): EP 90940 A

The **base** and **emitter regions** of an **npn bipolar transistor** are made by (a) depositing polySi (30) over a monocrystalline **Si** surface where base (42) and **emitter** (44) **regions** are to be formed; (b) implanting B ions into the polySi, near its interface with the monocrystalline

Si; (**c**) annealing to partly drive B ions into monocrystalline **Si**; (d) ion implanting As into the polySi; and (e) annealing to fully drive in B and As, forming **base** and **emitter regions**.

More specifically, **npn transistors** are formed in an IC by (i) providing an **Si** semiconductor body having monocrystalline **Si** regions sepd. by dielectric isolation regions; (ii) masking designated collector reach through regions while exposing **regions** for **emitter** and **intrinsic** and extrinsic **base regions**; (iii) forming doped polySi (24) on the surface ohmically contacting **extrinsic base regions**; (iv) removing polySi from above the mask for collector reach through; (v) forming an insulating layer and lithographically removing insulator and polySi from **regions** for **emitter** and **intrinsic base region**; (vi) forming an insulating layer (26) and selectively removing to form a sidewall on the first p-doped polySi layer; and (vii) continuing as (a)-(d).

High performance npn transistors are formed, with shallow narrow **base regions** having sufficient doping and width to avoid punch through.

Abstract (Equivalent): EP 90940 B

Method of forming the **emitter** and **base regions** (44,42) of an **NPN bipolar transistor** comprising: depositing a polycrystalline **silicon** layer (30) over a monocrystralline **silicon** surface in which the **base** and **emitter regions** (42,44) of said transistor are to be formed; ion implanting boron ions (32) into polycrystalline **silicon** layer (30) near the interface of polycrystalline **silicon** layer (30) with said monocrystalline **silicon**; forming a **silicon** dioxide capping layer (34) over polycrystalline **silicon** layer (30); annealing the layered structure to partially drive the boron ions (32) into said monocrystalline **silicon** (14); removing capping layer (34); ion implanting arsenic ions (38) into polycrystalline **silicon** layer (30); forming a **silicon** dioxide capping layer (40) over polycrystalline **silicon** layer (30); heating the layered structure to fully drive in the boron (32) and arsenic (38) to form **base** and **emitter regions** (42,44) of said transistor; and removing capping layer (40). (17pp)

Abstract (Equivalent): US 4431460 A

High performance npn bipolar transistor is made using a polycrystalline **Si** layer deposited over a monocrystalline **Si** surface in which **base** and **emitter regions** are to be formed. B ions are implanted into the polycrystalline layer near the interface with the monocrystalline layer and the structure annealed to drive B ions into the monocrystalline layer. As ions are implanted into the polycrystalline layer and annealing again carried out to fully drive in B and As to form the **base** and **emitter regions**.

Pref. the polycrystalline layer remains in the final structure as the contact to the **emitter region**. The polycrystalline layer is pref. 50-500 nm thick and the initial annealing is pref. carried out at 800-1000 deg. **C**.

A base is formed with sufficient width and doping to avoid punch-through. (10pp)t

31/3,AB/27 (Item 1 from file: 347)

07147780
SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

PUB. NO.: 2002-016159 [JP 2002016159 A]
PUBLISHED: January 18, 2002 (20020118)
INVENTOR(s): NAKAJIMA HIROOMI
NAGANO TAKAYUKI
INO KAZUMI
KATSUMATA YASUHIRO
ARAI HIDEAKI
FURUYA HIROMI
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 2000-194799 [JP 2000194799]
FILED: June 28, 2000 (20000628)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **high-performance** Bi-**CMOS** integrated circuit by a manufacturing method having fewer processes.

SOLUTION: In a Bi-**CMOS** integrated circuit constituted of a bipolar transistor structure and a **CMOS** structure, which are formed on an SOI substrate, the bipolar transistor structure is constituted of an **n-type** semiconductor region formed on a semiconductor layer on the SOI substrate, a collector region formed on this semiconductor **region**, a **base region** formed on the collector region, an insulating layer, which is formed on the **base region** and has an aperture, an **emitter region** formed in such a way as to have an exposed part on the bottom of the aperture on the upper layer part within the **base region** and a polycrystalline **Si** electrode formed in such a way as to bury the aperture in the insulating film.

31/3,AB/28 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06208680
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 11-150238 [JP 11150238 A]
PUBLISHED: June 02, 1999 (19990602)
INVENTOR(s): YOKOYAMA HIROAKI
APPLICANT(s): NEC CORP
APPL. NO.: 09-331200 [JP 97331200]
FILED: November 14, 1997 (19971114)

ABSTRACT

PROBLEM TO BE SOLVED: To realize compatibility for a short-channel **MOS** transistor and a **high-performance** Bip(bipolar) transistor, without increasing the number of processes for achieving high speed, coping with low voltage, for suppressing the fluctuations in characteristics, and to improve the yield of a product in **BiCMOS** SRAM.

SOLUTION: A Bip emitter electrode 14 is formed by the same conductive layer as MMOS and **PMOS** gate electrode 15 and 16. The conductive layer is set to a polycide structure, that is the laminated structure of

polycrystalline **silicon** 12a and metal silicide 13a with a high melt point, a sidewall **silicon** oxide film 19 is formed on the sidewall, the Bip emitter electrode 14 and the sidewall **silicon** oxide film 19 are used as a mask, and a **P-type** high concentration impurity region 21 that is the graft **base region** of a Bip transistor is formed in self-aligned manner. A GND potential line 24 is set to the single-layer structure of metal silicide 13b with the high molting point of Ti or W.

31/3,AB/29 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

03216658
SEMICONDUCTOR DEVICE

PUB. NO.: 02-192158 [JP 2192158 A]
PUBLISHED: July 27, 1990 (19900727)
INVENTOR(s): OGAWA KENJI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-011203 [JP 8911203]
FILED: January 19, 1989 (19890119)
JOURNAL: Section: E, Section No. 989, Vol. 14, No. 467, Pg. 124, October 11, 1990 (19901011)

ABSTRACT

PURPOSE: To obtain a transistor which is **high** in **performance** and applicable to many fields by a method wherein a gate electrode capable of optionally controlling a base in width is provided to a bipolar transistor.

CONSTITUTION: An **N**(sup +)-**type** collector region 2 doped high in concentration is provided to an **N-type** semiconductor substrate 1, a **base region** 3 which is thick but thin at its central part is provided to the surface of the substrate 1, and an **emitter region** 4 is provided to the surface layers of the thick parts of the **base region** 3 respectively. A gate oxide film 8 is provided in contact with the **emitter regions** 4 to insulate the semiconductor substrate 1 from an gate 9 which is to be built, and the gate 9 formed of polycrystalline **silicon** is provided thereon covering the whole thin part of the **base region** 3, and a collector electrode **C**, a base electrode B, an emitter electrode E, and a gate electrode G are provided to connect these regions with the outside respectively. By this setup, the relative diffusion depth difference between a base and an emitter can be strictly controlled making the diffusion of the base and the emitter small in depth, so that a semiconductor device of this design can be stabilized in characteristics.

31/3,AB/30 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

02547456
MANUFACTURE OF SEMICONDUCTOR INTEGRATED CIRCUIT

PUB. NO.: 63-164356 [JP 63164356 A]
PUBLISHED: July 07, 1988 (19880707)
INVENTOR(s): YONEDA TADANAKA
KAMEYAMA SHUICHI
KAJIYAMA MASAOKI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-312028 [JP 86312028]
FILED: December 26, 1986 (19861226)
JOURNAL: Section: E, Section No. 681, Vol. 12, No. 425, Pg. 97, November 10, 1988 (19881110)

ABSTRACT

PURPOSE: To lower collector resistance, and to obtain a bipolar transistor having good **high**-speed **performance** by forming regions having low resistivity into the emitter and collector contact forming regions of the bipolar transistor.

CONSTITUTION: An **n-type** epitaxial layer 23, etc., are shaped into the **n-p-n transistor** and **p-type** channel **MOS** transistor forming regions of a **p-type** 10ω-cm **silicon** substrate 20, and boron ions are implanted into an **n-type** channel **MOS** transistor forming region to shape a region 26 implanted with boron ions. Impurities in ion-implanted regions 24, 25, 26 are diffused through heat treatment at 1100 deg.**C** to form **n-type** regions 27, 28 having low resistivity, and a p well region 29 is shaped. Accordingly, collector resistance can be lowered. Since an **n-type** epitaxial layer 23 having high resistivity is formed under a **base** contact **region** 30 except an active **base region**, **base**-collector junction capacitance can be reduced, thus improving the high-frequency characteristics of the transistors.

31/3,AB/31 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

01976966
MANUFACTURE OF **BIPOLAR NPN TRANSISTOR**

PUB. NO.: 61-191066 [JP 61191066 A]
PUBLISHED: August 25, 1986 (19860825)
INVENTOR(s): HONMA AKIRA
APPLICANT(s): VICTOR CO OF JAPAN LTD [000432] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-032354 [JP 8532354]
FILED: February 20, 1985 (19850220)
JOURNAL: Section: E, Section No. 472, Vol. 11, No. 20, Pg. 88, January 20, 1987 (19870120)

ABSTRACT

PURPOSE: To manufacture a transistor characterized by low base resistance and high amplification factor readily, by introducing As or Sb in a part, which is to become an **emitter region** in an **N-type** **Si** substrate, performing wet oxidation at a low temperature, forming an oxide film, which is thicker than the other part, on the **emitter region**, and implanting B ions through said oxide film.

CONSTITUTION: In a part, which is to become an **emitter region** in an **N-type Si** substrate, As (a) or Sb is introduced at a specified concentration, and an implanted layer 12 is formed. An oxide

film 10 and photoresist 11 are removed, and wet oxidation is performed at a low temperature of about 900 deg.C. Then an oxide film 13, whose thickness is large only on the layer 12, is obtained. B ions are implanted in a **base region** through the oxide film 13. Then a part beneath the **emitter region** becomes a low concentration layer 15 and the other part becomes a high concentration layer 14. Then, thermal diffusion is **performed** at a **high** temperature (e.g., 1,050 deg.C). Then only B is diffused to the deep part since the diffusion coefficient of the B is larger than that of As or Sb. Low concentration base layers (8 and 9) are obtained only beneath the **emitter region**. Thus the transistor characterized by low base resistance and high amplification factor is simply obtained by one B implantation.

31/3,AB/32 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

01143474

FIELD EFFECT TRANSISTOR

PUB. NO.: 58-080874 [JP 58080874 A]
PUBLISHED: May 16, 1983 (19830516)
INVENTOR(s): YAMAMOTO YOSHIMICHI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-180097 [JP 81180097]
FILED: November 09, 1981 (19811109)
JOURNAL: Section: E, Section No. 190, Vol. 07, No. 174, Pg. 111, August 02, 1983 (19830802)

ABSTRACT

PURPOSE: To obtain a field effect transistor having less irregularity, small pinch- off voltage and a large conductance by forming a channel region on the surface of raised projection formed on the surface of a substrate.

CONSTITUTION: Photoresists 3, 3a are covered on the **regions** except the **base region** of an **N-P-N type transistor**, the gate region of a field effect transistor and a gate electrode producing region, and with the photoresists as masks boron ions are implanted, and an implantation layer 4 is formed on the surface of a **silicon** substrate 1. The region surrounded by implantation layers 6a, 6b becomes a raised projection 20 and a region operating as a channel layer. After the layers 6a, 6b are further respectively formed in recesses 21, 21, the photoresists 3, 3a, 5 are all removed, only the vicinity of the projection 20 is allowed to remain, and a photoresist 7 is again covered. After the implantation layer 8A is then formed, the photoresist 7 is removed, an annealing and a drive-in are **performed** in a **high** temperature furnace, thereby allowing the layers 6a, 6b, 4 to respectively become diffused layers 10a, 10b, 9. Thus, when inverse biase to be applied to the region 8 and the layers 10a, 10b is incereased, a depletion layer is expanded sequentially to the boundary lines (a), (b), (c), and when the region 8 is filled with the depletion layer, it is completely pinched off.

35/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5928986 INSPEC Abstract Number: A9813-6170T-014, B9807-2550B-024
Title: Ion implantation doping in SiC and its device applications
Author(s): Rao, M.V.; Gardner, J.; Edwards, A.; Papanicolaou, N.A.; Kelner, G.; Holland, O.W.; Ghezzo, M.; Kretchmer, J.
Author Affiliation: Dept. of Electr. & Comput. Eng., George Mason Univ., Fairfax, VA, USA
Journal: Materials Science Forum Conference Title: Mater. Sci. Forum (Switzerland) vol.264-268, pt.2 p.717-20
Publisher: Trans Tech Publications,
Publication Date: 1998 Country of Publication: Switzerland
CODEN: MSFOEP ISSN: 0255-5476
SICI: 0255-5476(1998)264/268:2L.717:IDDA;1-3
Material Identity Number: H866-98008
Conference Title: Silicon Carbide, III-Nitrides and Related Materials. 7th International Conference
Conference Sponsor: Linkoping Univ.; ABB Asea Brown Boveri; Cree Res.; Okmetik Oy; Epigress AB; et al
Conference Date: 31 Aug.-5 Sept. 1997 Conference Location: Stockholm, Sweden
Language: English
Abstract: Our latest ion-implantation results on SiC are presented. We have **performed** nitrogen and phosphorous (**N/P**) co-implantations to obtain very high **n-type** carrier concentrations, **Si** and **C** bombardments for compensating **n-type** SiC, and V-implantation for compensating **p-type** SiC. We have also performed N and Al implantations directly into V-doped semi-insulating 6H-SiC substrates. **Vertical p-n** junction diodes were made by selective area N, P, and N/P implantations into **p-type** epitaxial layers grown on 6H-SiC substrates.
Subfile: A B A

35/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

04294521 INSPEC Abstract Number: A9302-8115G-019, B9301-0510D-049
Title: Molecular-beam epitaxial growth and characterization of **silicon** -doped AlGaAs and GaAs on (311)A GaAs substrates and their device applications
Author(s): Li, W.Q.; Bhattacharya, P.K.; Kwok, S.H.; Merlin, R.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., Michigan Univ., Ann Arbor, MI, USA
Journal: Journal of Applied Physics vol.72, no.7 p.3129-35
Publication Date: 1 Oct. 1992 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
U.S. Copyright Clearance Center Code: 0021-8979/92/193129-07$04.00
Language: English
Abstract: The possibility of reliable and reproducible **p-type** doping of (311)A GaAs by **Si** during molecular-beam epitaxial growth and the application of such doping in the realization of **high-performance** electronic devices have been investigated. It is seen that **p-type** doping up to a free hole concentration of 4*10/sup 19/ cm/sup -3/ can be obtained under conditions of low As/sub 4/ flux and high (>or=660 degrees **C**) growth temperatures. **n-type**

doping up to a level of 1*10/sup 19/ cm/sup -3/ is obtained at low (<or=500 degrees **C**) growth temperature and high As/sub 4/ flux. The **p-type** doping is extremely reproducible and the incorporation of **Si** atoms into electrically active As sites is at least 95%. The doping behavior has been studied and confirmed by Raman spectroscopy. **n-p-n** heterojunction **bipolar transistors** grown by all **Si** doping exhibit excellent current voltage characteristics and a common emitter current gain beta =240. Doped channel **p-type** heterojunction field-effect transistors have transconductance g/sub m/=25 mS/mm.

Subfile: A B

35/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

04241542 INSPEC Abstract Number: B9211-2560J-005

Title: The use of an interface anneal to control the base current and emitter resistance of **p-n-p** **polysilicon** emitter **bipolar transistors**

Author(s): Post, I.R.C.; Ashburn, P.

Author Affiliation: Dept. of Electron. & Comput. Sci., Southampton Univ., UK

Journal: IEEE Electron Device Letters vol.13, no.8 p.408-10

Publication Date: Aug. 1992 Country of Publication: USA

CODEN: EDLEDZ ISSN: 0741-3106

U.S. Copyright Clearance Center Code: 0741-3106/92/$03.00

Language: English

Abstract: The effects of an interface anneal on the electrical characteristics of **p-n-p** **polysilicon**-emitter **bipolar transistors** are reported. For devices with a deliberately grown interfacial oxide layer, an interface anneal at 1100 degrees **C** leads to a factor of 15 increase in base current, and a factor of 2.5 decrease in emitter resistance, compared with an unannealed control device. These results are compared with identical interface anneals **performed** on **n-p-n** devices, and it is shown that the increase in base current for p-n-p devices is considerably smaller than that for the n-p-n devices. This result is explained by the presence of fluorine in the p-n-p devices, which accelerates the breakup of the interfacial layer.

Subfile: B

35/3,AB/4 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04341188

E.I. No: EIP96023020855

Title: MBE growth and device applications of lattice-matched and strained heterostructures on (n11)-oriented and patterned substrates

Author: Bhattacharya, Pallab

Corporate Source: Univ of Michigan, Ann Arbor, MI, USA

Conference Title: Proceedings of the 1994 1st International Workshop on Growth, Characterization and Exploitation of Epitaxial III-V Compound Semiconductor on Novel Index Surfaces

Conference Location: Trento, Italy Conference Date: 19941204-19941207

E.I. Conference No.: 44283

Source: Microelectronics Journal v 26 n 8 Dec 1995. p 887-896

Publication Year: 1995
CODEN: MICEB9 ISSN: 0026-2692
Language: English
Abstract: The epitaxy of lattice-matched and strained semi-conducting films on patterned and misoriented substrates has led to new growth phenomena, material properties and device applications. Our work on InP- and GaAs-based heterostructures on (111)- and (311)-oriented substrates and strained heterostructures on planar and patterned (small area) substrates is described in this paper. The possibility of reliable and reproducible **p-type** doping of (311)A GaAs by **Si** during molecular-beam epitaxial growth and the application of such doping in the realization of **high-performance** electronic devices have been investigated. It is seen that **p-type** doping up to a free hole concentration of 4 multiplied by 10**1**9 cm** minus **3 is obtained at low (less than equivalent to 500 degree **C**) growth temperature and high As//4 flux. The incorporation of **Si** atoms into electrically active As sites is at least 95%. **n-p-n** heterojunction **bipolar transistors** grown by all-**Si** doping exhibit excellent current voltage characteristics and a common emitter current gain beta equals 240. Doped channel **p-type** heterojunction field-effect transistors have transconductance g//m equals 25 mS/mm. We have experimentally and theoretically studied piezoelectric field effects in InP-based In//xGa//1// minus //xAs/In//0//.//5//2Al//0//.//4//8As pseudomorphic quantum wells grown by molecular-beam epitaxy on (111)B InP substrates. The electro-optic coefficients of this material were measured and found to be much larger than that of GaAs. We have also investigated the consequences of altered growth modes on the epitaxy of highly strained InGaAs on patterned small area (001) GaAs substrates.
Al//0//.//1//5Ga//0//.//8//5As/In//0//.//2//5Ga//0//.//7//5As pseudomorphic modulation-doped field-effect transistors and strained In//xGa//1// minus //xAs/GaAs p-i-n photodiodes have been fabricated on patterned (100)GaAs substrates and characterized. Compared with devices made on planar substrates, small area growth improves the dc transconductance by 40% and current gain cutoff frequency by 50% in the transistors. Photodiodes grown in small recesses (approximately 30 mu m) exhibit 2-4 times higher quantum efficiency than those on planar substrates. (Author abstract) 33 Refs.

35/3,AB/5 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

03535368 Genuine Article#: PK458 Number of References: 54
Title: CHARGE-INJECTION THEORY OF BIPOLAR JUNCTION TRANSISTORS (Abstract Available)
Author(s): RODE DL
Corporate Source: WASHINGTON UNIV,DEPT ELECT ENGN/ST LOUIS//MO/63130
Journal: JOURNAL OF APPLIED PHYSICS, 1994, V76, N7 (OCT 1), P4173-4183
ISSN: 0021-8979
Language: ENGLISH Document Type: ARTICLE
Abstract: A physical theory of the bipolar junction transistor which provides closed-form solutions for current/voltage relations for generalized bias conditions is introduced. Included are the new concepts of emitter and collector collection efficiency. Both **emitter** and collector **regions** are treated symmetrically to allow for accurate treatment of operation in both the saturation region and the forward-active region, as well as the reverse-active region. There are six components each of emitter and collector current, resulting from inclusion of emitter injection efficiency, surface recombination at the pn junction peripheries, and bulk base

recombination as well as finite minority-carrier collection efficiency. Direct comparison between theory and experiment over the entire transistor operating range from deep saturation where I(**C**) = 0 continuously into the forward-active region where V(CE) is much greater than the thermal voltage V(T) shows excellent agreement.

35/3,AB/6 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

01733958 Genuine Article#: HW654 Number of References: 34
Title: EFFECTS OF HEAVY DOPING ON NUMERICAL SIMULATIONS OF GALLIUM-ARSENIDE BIPOLAR-TRANSISTORS (Abstract Available)
Author(s): TOMIZAWA M; ISHIBASHI T; BENNETT HS; LOWNEY JR
Corporate Source: NIPPON TELEGRAPH & TEL PUBL CORP,LSI LABS/ATSUGI/KANAGAWA 24301/JAPAN/; NATL INST STAND & TECHNOL,DIV SEMICOND ELECTR,ELECTR & ELECT ENGN LAB/GAITHERSBURG//MD/20899
Journal: SOLID-STATE ELECTRONICS, 1992, V35, N6 (JUN), P865-874
Language: ENGLISH Document Type: ARTICLE
Abstract: Using the best available physical models is essential for predictive numerical simulations of advanced, **high performance** GaAs transistors. Among the many input parameters for numerical simulations, the effective intrinsic carrier concentrations, n(ie), minority carrier mobilities, mu, and recombination lifetimes, tau, are very critical parameters. The results from recent theoretical calculations for n(ie) were implemented into a two-dimensional, drift-diffusion simulator for GaAs transistors. In order to compare predicted and measured d.**c**. common emitter gains, **NPN** GaAs homojunction **bipolar transistors** with different but heavily doped bases and similarly doped emitters that have widths between 0.1 and 0.45-mu-m were fabricated by molecular beam epitaxy. The predicted gains of 8, 25, 46, 72 for these transistors agreed very well with their measured gains of 9, 22, 42 and 70 at high current, respectively. Without using the new theoretical data for n(ie) but setting n(ie) equal everywhere to the intrinsic carrier concentration, n(i), the predicted pins became 4, 14, 27 and 35, respectively. Sensitivity analyses on mobilities, lifetimes, and n(ie) showed that physically correct n(ie) values are quantitatively very important for predictive simulations of GaAs bipolar transistors.

35/3,AB/7 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01336219 AADC333010
EPITAXIAL ALIGNMENT OF POLYCRYSTALLINE **SILICON** AND ITS IMPLICATIONS FOR ANALOGUE BIPOLAR CIRCUITS
Author: WILLIAMS, JOHN DILWYN
Degree: PH.D.
Year: 1992
Corporate Source/Institution: UNIVERSITY OF SOUTHAMPTON (UNITED KINGDOM) (5036)
Source: VOLUME 55/01-C OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 278.

This thesis investigates the conditions which lead to the epitaxial alignment of **n-type** and **p-type** polycrystalline **silicon** layers deposited on **silicon**, which are subjected to

either a single emitter diffusion (single diffused) or consecutive base and emitter diffusions (double diffused). A wide range of diffusion conditions is considered, covering both rapid thermal and furnace diffusion in the temperature range 950-1200$\sp\circ$**C**. In contrast the sheet resistances of single and double diffused **p-type polysilicon** layers are found to be similar within this temperature range.

Estimates are made of the time to break up the interfacial oxide and the time to vertically epitaxially align **n-type polysilicon** at different temperatures, and activation energies of 4.9eV and 4.7eV respectively obtained. In **n-type polysilicon**, the epitaxial regrowth is dominated by the time to break the interfacial oxide layer, whereas in BF$\sb2\sp+$ implanted **polysilicon** it is dominated by the time to vertically epitaxially align the **polysilicon.**

A theoretical model is proposed for the process of epitaxial alignment, which accounts for the observed linear epitaxial alignment rates and the measured activation energy of 4.7eV. In addition, the author proposes an alternative to the standard theoretical models for the break up of the interfacial oxide. It is proposed that both oxide break up and vertical epitaxial alignment are dominated by the self-diffusion of **silicon,** which has a theoretical activation energy of 4.86eV.

NPN phosphorus implanted **bipolar transistors** are fabricated with either a **polysilicon** contacted emitter or an epitaxially aligned single crystal **silicon** emitter. The current gain for the **polysilicon** emitter transistor is found to be $\sim$1.6 times higher than that of the epitaxially aligned emitter due to the blocking of holes at the **polysilicon/silicon** interface, which results in lower base current. Calculations are made to illustrate the extent that the increased gain of the **polysilicon** emitter transistor can be traded for a lower base resistance. The implications of this for **high** -frequency, analogue circuit **performance** are discussed. (Abstract shortened by UMI.)

35/3,AB/8 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01448871 JICST ACCESSION NUMBER: 92A0156476 FILE SEGMENT: JICST-E
Bipolar-Complementary-Metal-Oxide-Semiconductor(BiCMOS) Technology with **Polysilicon** Self-Aligned Bipolar Devices.
KIM K S (1); NAM K S (1); AN C (2)
(1) Electronics and Telecommunication Research Inst., Chungnam, KOR; (2) Sogang Univ., Seoul, KOR
Jpn J Appl Phys Part 1, 1991, VOL.30,NO.10, PAGE.2459-2465, FIG.14, TBL.2, REF.5
JOURNAL NUMBER: G0520BAE ISSN NO: 0021-4922
UNIVERSAL DECIMAL CLASSIFICATION: 621.382 SS 621.382 MIS 621.382.3
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: An advanced **bipolar-complementary-metal- oxide-semiconductor(BiCMOS)** technology providing uncompromised **high-performance,** double **polysilicon** self-aligned(PSA) **n-p-n bipolar** and 1.25Mm gate length **CMOS** transistors is described. The **polysilicon** self-aligned-**BiCMOS** technology(PSA-**BiCMOS**) is intended for high-speed logic circuit operation at 5V, where a high level of circuit integration and power consumption is involved. Features

include **vertical n-p-n transistors** with a self-aligned **n+ polysilicon emitter** and **p+ polysilicon** base. The **CMOS** transistor features n+ **polysilicon** gates and lightly doped drain(LDD) **NMOSFET.** A process simulator, Stanford University process engineering models(SUPREM III) and device simulator, Poisson and continuity equation solver(PISCES II) were used to optimize the process steps and to enhance device characteristics, respectively. The performance of N- and **PMOS** transistors is comparable to those of a conventional **CMOS** process. The driving capability of **CMOS** and PSA- **BiCMOS** was compared according to fan-out. Compared to **CMOS**, PSA-**BiCMOS** has good driving capability from about 2.5 fan-out and PSA-**BiCMOS** with 1.25Mm N- and **PMOS** transistors and a bipolar transistor with 2Mm emitter width exhibits an average ring oscillator delay of 6.25ns/stage at 1pF load capacitance at 5V. (author abst.)

35/3,AB/9 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

12440912 PASCAL Number: 96-0097410
MBE growth and device applications of lattice-matched and strained heterostructures on (n11)-oriented and patterned substrates
Novel index semiconductor surfaces
PALLAB BHATTACHARYA
HENINI Mohamed, ed
University Michigan, dep. electrical english computer sci., solid state electronics laboratory, Ann Arbor MI 48109-2122, USA
University Nottingham, physics dep., Nottingham NG7 2RD, United Kingdom
International workshop on growth, characterization and exploitation of epitaxial III-V compound semiconductor on novel index surfaces, 1 (Trento ITA) 1994-12-04
Journal: Microelectronics journal, 1995, 26 (8) 887-896
Language: English
The epitaxy of lattice-matched and strained semi-conducting films on patterned and misoriented substrates has led to new growth phenomena, material properties and device applications. Our work on InP- and GaAs-based heterostructures on (111)- and (311)-oriented substrates and strained heterostructures on planar and patterned (small area) substrates is described in this paper. The possibility of reliable and reproducible **p-type** doping of (311)A GaAs by **Si** during molecular-beam epitaxial growth and the application of such doping in the realization of **high-performance** electronic devices have been investigated. It is seen that **p-type** doping up to a free hole concentration of 4x10 SUP 1 SUP 9 cm SUP - SUP 3 is obtained at low (<=500 Degree **C**) growth temperature and high As SUB 4 flux. The incorporation of **Si** atoms into electrically active As sites is at least 95%. **n-p-n** heterojunction **bipolar transistors** grown by all-**Si** doping exhibit excellent current voltage characteristics and a common emitter current gain beta =240. Doped channel **p-type** heterojunction field-effect transistors have transconductance g SUB m = 25 mS/mm. We have experimentally and theoretically studied piezo-electric field effects in InP-based In SUB x Ga SUB 1 SUB - SUB x As/In SUB 0 SUB . SUB 5 SUB 2 Al SUB 0 SUB . SUB 4 SUB 8 As pseudomorphic quantum wells grown by molecular-beam epitaxy on (111)B InP substrates. The electro-optic coefficients of this material were measured and found to be much larger than that of GaAs. We have also investigated the consequences of altered growth modes on the epitaxy of highly strained InGaAs on patterned small

area (001) GaAs substrates. Al SUB 0 SUB . SUB 1 SUB 5 Ga SUB 0 SUB . SUB 8 SUB 5 As/In SUB 0 SUB . SUB 2 SUB 5 Ga SUB 0 SUB . SUB 7 SUB 5 As pseudomorphic modulation-doped field-effect transistors and strained In SUB x Ga SUB 1 SUB - SUB x As/GaAs p-i-n photodiodes have been fabricated on patterned (100)-GaAs substrates and characterized. Compa

35/3,AB/10 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008649384
WPI Acc No: 1991-153413/199121
Related WPI Acc No: 1991-153401; 1991-153412; 1991-153414; 1991-226571; 1991-249775
XRAM Acc No: C95-075052
XRPX Acc No: N95-127074

Monolithic IC with **higher** speed **performance** - has PIN photodiode and **n-p-n bipolar transistor** on the same substrate

Patent Assignee: HAMAMATSU PHOTONICS KK (HAMM)
Inventor: KYOMASU M; NAKAMURA H; OKAJIMA K; SAHARA M

Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 3089562	A	19910415	JP 89226306	A	19890831	199121	B
US 5410175	A	19950425	US 90576065	A	19900831	199522	
			US 92899591	A	19920618		

Priority Applications (No Type Date): JP 89226306 A 19890831; JP 89226305 A 19890831; JP 89226307 A 19890831; JP 89226308 A 19890831; JP 89226309 A 19890831; JP 89284191 A 19891031; JP 89284192 A 19891031
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5410175	A		31	H01L-027/14	Cont of application US 90576065

Abstract (Basic): US 5410175 A

Semiconductor device comprises: (a) heavily doped **p-type** substrate, lightly doped **p-type** epitaxial layer, and **n-type** epitaxial layer; (b) doped **n-type** layer formed in the surface of a predetermined region of the lightly doped **p-type** epitaxial layer, the heavily doped substrate serving as a P layer and the lightly doped layer as I layer and the **n-type** layer as N layer of a PIN photodiode; and (**c**) electronically active element in the **n-type** layer near the predetermined region.

Also claimed is: (i) the device in which the substrate is **n-type**; (ii) the device with electrode layers; and (iii) the PIN photodiode.

The electronically active element comprises an **n-p-n bipolar transistor** of **p-type** base, **n-type emitter** formed by doping the **n-type** epitaxial layer and an **n-type** collector. The substrate and epitaxial layers are **Si**. Part of the **n-type** layer in the predetermined region is left as an electrode layer and a **silicon** oxide film of the same thickness is formed by oxidising the periphery region.

USE - Monolithic IC with PIN photodiode.

ADVANTAGE - **Higher** speed **performance**.

Dwg.1/12

35/3,AB/11 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004830202
WPI Acc No: 1986-333543/198651
XRAM Acc No: C86-144481
XRPX Acc No: N86-248727
Bipolar and **CMOS**-transistors are constructed on a single substrate - without using oxide to isolate the areas
Patent Assignee: SIEMENS AG (SIEI)
Inventor: JACOBS E P
Number of Countries: 008 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 204979	A	19861217	EP 86106486	A	19860513	198651	B
JP 61279171	A	19861209				198703	
US 4717686	A	19880105	US 86869306	A	19860602	198803	
EP 204979	B	19890329				198913	
DE 3662627	G	19890503				198919	

Priority Applications (No Type Date): DE 3519790 A 19850603
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 204979	A	E	22		
Designated States (Regional): AT DE FR GB IT NL					
EP 204979	B	G			
Designated States (Regional): AT DE FR GB IT NL					

Abstract (Basic): EP 204979 B
npn-Bipolar transistors are mfd. on a single **p-type** (100) **Si**-substrate (area A), while at the same time, in other areas (B,**C**) complementary **MOS**-transistors are constructed.
Process uses **n-type** wells which also serve as the collector-diffusions in the **npn-transistors**. A deep diffusion (6) provides a guard-ring around the **npn-transistor** avoiding the occurrence of latch-up. A buried n(+) diffusion and a 3 micron thick epitaxial **p-type** layer when used, further improve the **npn-transistor**.
USE/ADVANTAGE - Allows bipolar transistors to be mfd. on the same die as **CMOS**-devices without requiring oxide-isolation as in current amount This feature allows better **npn-transistor** characteristics. The reduced collector-resistance of the construction reduces the danger of latch-up. The process can be used for the mfr. of VLSI-devices requiring **high** speed **performance**. (22pp Dwg.No.14/14)
Abstract (Equivalent): EP 204979 B
Method of simultaneously producing bipolar (A) and complementary **MOS** (**CMOS**) transistors (B, **C**) on a common **silicon** substrate in which n-doped tubs are produced in the p-doped **silicon** substrate for receiving the p-channel **transistors** (**C**) and isolated **npn bipolar transistors** (A) are laid down in the n-doped tubs, the **n-type** tub forming the collector of the transistor (A) and in which the **n-type** tubs cover buried n+-doped zones which are connectd by deeply extending collector connections in the bipolar transistor region (A), characterized by the sequence of following

process steps: (a) production of the buried n+-doped zones in the p-doped susbtrate by implantation of n-doping ions after prior masking of the remaining regions, (b) application of a p-doped epitaxial layer over the entire surface, (c) productien of a double-isolation layer composed of **silicon** oxide and **silicon** nitride over the entire surface, (d) establishment of the regions for the deeply extending collector connection by a deep implantation with n-doping ions after prior structuring of the **silicon** nitride layer by photolithography; (e) production of the **n-type** tubs in the substrate by implantation of n-doping ions after stripping the **silicon** nitride structures above the **n-type** tub regions; (f) diffusion of the implanted n-doping ions into the substrate and simultaneous oxidation of the surface in the **n-type** tub regions, (g) carrying out of a deep implantation of boron ions to produce the region of the channel zone, remote from the surface, of the n-channel transistors (B) after removing the **silicon** nitride structures, the oxide acting as a mask, (h) application of a double layer composed of **silicon** oxide and **silicon** nitride and suitable structuring of the **silicon** nitride layer for the subsequent local oxidation (LOCOS), (i) carrying out of a boron ion implantation to dope the field oxide regions of the n-channel transistors after prior photoresist masking of the remaining regions, (j) production of th

Abstract (Equivalent): US 4717686 A

For mfr. of **vertical NPN** and lateral **PNP** **bipolar transistors** and complementary **MOS** transistors, a P-doped **Si** substrate is coated with **Si** dioxide and **Si** nitride, the latter layer being restructured. Deep collector region is produced in the substrate by implantation of n-doping ions, **Si** nitride is removed, and n-doping ions are implanted to form n wells in the removal regions. The n-doping ions are diffused in and surfaces of n-wells are oxidised to form masks, through which B ions are implanted. Double layer is re-applied and **Si** nitride is structured to open active regions, selected regions being masked. B ions are implanted through the mask to dope field oxide regions, mask is removed and substrate is locally oxidised to form field oxide regions.

Photo-resist mask defines base of bipolar transistor and B ions are implanted before removal and oxidation to form gate oxide. B ions are implanted over surface to dope N and P channels of **MOS** transistors and gate material is deposited for them. **Si** dioxide is deposited as intermediate oxide, n-doping and B ions are selectively implanted.

ADVANTAGE - **Vertical** and lateral **transistors** and **MOS** transistors are mfd. on one chip. (10pp)1

35/3,AB/12 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07340150
SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR

PUB. NO.: 2002-208641 [JP 2002208641 A]
PUBLISHED: July 26, 2002 (20020726)
INVENTOR(s): KURANOUCHI ATSUSHI
APPLICANT(s): SONY CORP
APPL. NO.: 2001-001993 [JP 20011993]
FILED: January 10, 2001 (20010110)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **high-performance** and **high** -reliability semiconductor device and the manufacturing method thereof, wherein there are mounted on a single semiconductor substrate a bipolar transistor for high-withstanding- voltage applications and a bipolar transistor for high-speed applications which have respective epitaxial-base structures to mix them with each other, and their optimal maximum power-supply voltages are realized respectively and their respective high breakdown voltage characteristic and high-speed characteristics can be displayed fully.

SOLUTION: There are mounted on a **P-type Si** substrate 10 a **vertical NPN bipolar transistor** 50a for high-speed applications and a **vertical NPN bipolar transistor** 50b for high breakdown voltage applications which have respective epitaxial-base structures to mix them with each other. Since a recessed cavity is formed on the surface of an **N-type** collector layer 14a of the **vertical NPN bipolar transistor** 50a for high-speed applications, the thickness of its **N-type** collector layer 14a is made smaller than the thickness of an **N-type** collector layer 14b of the **NPN bipolar transistor** 50b for high breakdown voltage applications.

39/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5388567 INSPEC Abstract Number: A9622-8115G-041, B9611-0510D-130
Title: Heterojunction bipolar transistors with low temperature Be-doped base grown by CBE
Author(s): Munns, G.O.; Chen, W.L.; Haddad, G.I.
Author Affiliation: Solid State Electron. Laboratory, Michigan University, Ann Arbor, MI, USA
Journal: Journal of Crystal Growth Conference Title: J. Crystalline Growth (Netherlands) vol.164, no.1-4 p.476-84
Publisher: Elsevier,
Publication Date: July 1996 Country of Publication: Netherlands
CODEN: JCRGAE ISSN: 0022-0248
SICI: 0022-0248(199607)164:1/4L.476:HBTW;1-O
Material Identity Number: J037-96016
U.S. Copyright Clearance Center Code: 0022-0248/96/$15.00
Conference Title: Chemical Beam Epitaxy and Related Growth Techniques 1995. Fifth International Conference
Conference Date: 14-16 Aug. 1995 Conference Location: La Jolla, CA, USA
Language: English
Abstract: Growth of highly doped **p-type** InGaAs is required for low contact resistivity demanded by **high performance** microwave devices. Increasing the doping level in the base of HBTs is known to be reflected in better unity power gain cut-off frequency. Low temperature growth has been shown to significantly enhance the maximum doping levels obtainable in **carbon**-doped bases of **Npn transistors** [C.J. Palmstrom et al., Appl. Phys. Lett. 64 (1994) 3139]. However, low temperature growth of Be-doped InGaAs has been reported to significantly degrade surface morphology of CBE grown material [T.K. Uchida et al., J. Appl. Phys. 29 (1990) L2146]. In this study the opposite effect was found. As the growth temperature was lowered, the surface morphology improved. Co-optimized normal growth temperature of InP and InGaAs has been previously determined to be 525 degrees **C** while the low temperature is approximately 460 degrees **C**. Growth was performed using a Varian Gen II CBE reactor using triethylgallium, trimethylindium, 100% phosphine and 100% arsine as source materials. Elemental **Si** and Be were used as n- and **p-type** dopants. A factor of 2 improvement in the doping level was seen with a maximum level of 6.10/sup 19/ cm/sup -3/ measured by the Van der Pauw-Hall technique. A marked improvement in the surface morphology and X-ray spectra accompanies this reduction in temperature from a rough surface at normal temperature to specular at low temperature. SHBTs have been grown using both low temperature base structures and normal temperature base structures. The contact resistivity for the base improves by an order of magnitude (to 4.10/sup -6/ Omega .cm/sup 2/) and the sheet resistance improves by a factor of 6 (to 324 Omega / Square Operator). DC current gains of 25, a common emitter breakdown of 6 V and a common base breakdown of 9 V are obtained. The unity current cut-off frequency for these heavily doped structures is above 90 GHz for a 4*4 mu m emitter geometry and the unity power gain cut-off frequency improves by more than a factor of 2 when compared to the lower-doped structure to above 100 GHz. Detailed X-ray investigation of the bulk low temperature InGaAs base and the InGaAs/InP interface are presented as are explicit HBT structures, s-parameter modeling of the HBT, and **high** frequency **performance** limitations.

Subfile: A B
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39/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2004 Institution of Electrical Engineers. All rts. reserv.

03854540 INSPEC Abstract Number: B91024546
Title: **SiGe**-base **PNP transistors** fabricated with **n**-**type** UHV/CVD LTE in a 'No Dt' process
Author(s): Harame, D.L.; Stork, J.M.C.; Meyerson, B.S.; Crabbe, E.F.; Patton, G.L.; Scilla, G.J.; de Fresart, E.; Bright, A.A.; Stanis, C.; Megdanis, A.C.; Manny, M.P.; Petrillo, E.J.; Dimeo, M.; McIntosh, R.C.; Chan, K.K.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Conference Title: 1990 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.90CH2874-6) p.47-8
Publisher: IEEE, New York, NY, USA
Publication Date: 1990 Country of Publication: USA xvii+143 pp.
U.S. Copyright Clearance Center Code: CH2874-6/90/0000-0047$01.00
Conference Sponsor: IEEE; Japan Society Appl. Phys
Conference Date: 4-7 June 1990 Conference Location: Honolulu, HI, USA
Language: English
Abstract: Experimental results are presented on the use of **N-type** ultrahigh-vacuum/chemical vapor deposition (UHV/CVD) low-temperature epitaxy (LTE) to deposit thin (45 nm), heavily doped (1*10/sup 19/ cm/sup -3/) **SiGe** films to form the base of **PNP transistors**. To take full advantage of epitaxial base technology, the thermal cycles following the base deposition that cause dopant diffusion and relaxation of highly strained layers must be eliminated. This objective is met by a novel process using PECVD insulators and UHV/CVD LTE emitter deposition to limit the temperature following the base deposition to 550 degrees **C** . This is essentially a 'No Dt' process in the sense that the effective dopant diffusion length Dt is negligible at this temperature. An advanced double-**polysilicon** bipolar structure was modified to fabricate non-self-aligned small-geometry transistors. Both DC and AC measurements were used to characterize the devices, confirming the presence of a large valence band offset at the base-collector junction. The resulting barrier to minority carrier transport caused additional charge storage in the neutral base and limited the peak cutoff frequency to 15 GHz independent of collector doping. The results demonstrate the impact of the valence band offset of **SiGe** heterojunctions on the **performance** of **PNP transistors**.
Subfile: B

39/3,AB/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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03495010
E.I. Monthly No: EI9210124432
Title: A **high-performance** 0.5- mu m **BiCMOS** technology for fast 4-Mb SRAM's.
Author: Hayden, James D.; Mele, Thomas C.; Perera, Asanga H.; Burnett, David; Walczyk, Fred W.; Lage, Craig S.; Baker, Frank K.; Woo, Michael; Paulson, Wayne; Lien, Mitch; See, Yee-Chaung; Denning, Dean; Cosentino, Stephen J.

Source: IEEE Transactions on Electron Devices v 39 n 7 Jul 1992 p 1669-1679
Publication Year: 1992
CODEN: IETDAI ISSN: 0018-9383
Language: English
Abstract: A **high-performance** 0.5- mu m **BiCMOS** technology has been developed for a fast 4-Mb SRAM class of circuits. Three layers of **polysilicon** are used to achieve a compact four-transistor SRAM bit cell size of less than 20 mu m**2 by creating self-aligned bit-sense and V//s//s contacts. A WSi//x polycide **emitter n-p-n transistor** with an emitter area of 0.8 multiplied by 2.4 mu m**2 provides a peak cutoff frequency (f//T) of 14 GHz with a collector-emitter breakdown voltage (BV//**C**//E//O) of 6.5 V. A selectively ion-implanted collector (SIC) is used to compensate the base channeling tail in order to increase f//T and knee current without significantly affecting collector-substrate capacitance. ECL gate delays as fast as 105 ps can be obtained with this process. 11 Refs.

39/3,AB/4 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

01574469 Genuine Article#: HJ059 Number of References: 24
Title: DOPANT INCORPORATION IN GAAS AND ALGAAS GROWN BY MOMBE FOR HIGH-SPEED DEVICES (Abstract Available)
Author(s): ABERNATHY CR; REN F; PEARTON SJ; SONG J
Corporate Source: AT&T BELL LABS/MURRAY HILL//NJ/07974; MIT/CAMBRIDGE//MA/02139
Journal: JOURNAL OF ELECTRONIC MATERIALS, 1992, V21, N3 (MAR), P323-327
Language: ENGLISH Document Type: ARTICLE
Abstract: Continued improvement in GaAs/AlGaAs device technology requires higher doping levels, both to reduce parasitics such as source resistances, and to enhance speed in devices such as the heterostructure bipolar transistor (HBT). In this paper we will discuss doping issues which are critical to **high** speed **performance**. In particular, we will focus on doping of GaAs and AlGaAs using **carbon** as the acceptor and Sn as the donor. Due to the unique growth chemistry of metalorganic molecular beam epitaxy (MOMBE), both of these impurities can be used to achieve high doping levels when introduced from gaseous sources such as trimethylgallium (TMG) or tetraethyltin (TESn). Comparison of SIMS and Hall measurements show that both elements give excellent electrical activation to 1.5 x 10(19) cm-3 for Sn and 5 x 10(20) cm-3 for **C**. More importantly, we have found that both impurities can be used to achieve high quality junctions, indicating that little or no diffusion or segregation is occurring during growth. Because of the excellent incorporation behavior of these dopants, we have been able to fabricate a wide range of devices including field effect transistors (**FETs**), high electron mobility **transistors** (HEMTs), and **Pnp** HBTs whose **performance** equals or exceeds that of similar devices grown by other techniques. In addition to these results, we will briefly discuss the key differences in growth kinetics which allow such abruptness and high doping levels to be achieved more readily in MOMBE than in other growth techniques.

39/3,AB/5 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

10209884 PASCAL Number: 92-0415786
A **high-performance** 0.5- mu m **BiCMOS** technology for fast 4-Mb SRAM's
HAYDEN J D; MELE T C; PERERA A H; BURNETT D; WALCZYK F W; LAGE C S; BAKER F K; WOO M; PAULSON W; YEE-CHAUNG SEE; DENNING D; COSENTINO S J
Motorola Inc., advanced products res. development laboratory, Austin TX 78721, USA
Journal: IEEE transactions on electron devices, 1992, 39 (7) 1669-1679
Language: English
A **high-performance** 0.5 mu m **BiCMOS** technology has been developed for a fast 4-Mb SRAM class of circuits. Three layers of **polysilicon** are used to achieve a compact four transistor SRAM bit cell size of less than 20 mu m SUP 2 by creating self-aligned bit-sense and V SUB s SUB s contacts. A WSi SUB x polycide **emitter n-p-n transistor** with an emitter area of 0.8x2.4 mu m SUP 2 provides a peak cutoff frequency (f SUB T) of 14 GHz with a collector-emitter breakdown voltage (BV SUB **C** SUB E SUB O) of 6.5 V

39/3,AB/6 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013085246
WPI Acc No: 2000-257118/200022
Related WPI Acc No: 2000-464045; 2001-389221; 2002-401739; 2003-532399
XRAM Acc No: C00-078650
XRPX Acc No: N00-191117
Thin epitaxial process for high speed complementary **bipolar/complementary metal oxide semiconductor** involves heating, depositing two thin intrinsic cap layers and performing gas purging cycle
Patent Assignee: BURR BROWN CORP (BURR-N)
Inventor: BAO K X; DROBNY V F
Number of Countries: 021 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200014795	A1	20000316	WO 99US19370	A	19990823	200022	B
EP 1116269	A1	20010718	EP 99945182	A	19990823	200142	
			WO 99US19370	A	19990823		
TW 425604	A	20010311	TW 99115124	A	19990902	200143	
JP 2002524876	W	20020806	WO 99US19370	A	19990823	200266	
			JP 2000569442	A	19990823		

Priority Applications (No Type Date): US 98149353 A 19980908
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200014795	A1	E	45	H01L-021/8238	
	Designated States (National): JP				
	Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE				
EP 1116269	A1	E		H01L-021/8238	Based on patent WO 200014795
	Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE				
TW 425604	A			H01L-021/20	
JP 2002524876	W		55	H01L-021/331	Based on patent WO 200014795

Abstract (Basic): WO 200014795 A1
Abstract (Basic):
NOVELTY - An epitaxial layer is formed on a **p type**

silicon substrate by subsequent heating steps before a first thin intrinsic epitaxial cap layer is formed. A purge gas cycle is performed before forming the second thin epitaxial cap layer and is followed by a second gas purging cycle and an N- epitaxial layer is deposited.

DETAILED DESCRIPTION - An epitaxial layer is formed on a **silicon** substrate (30) having a P+ field layer region in the major surface involves (a) loading the substrate in a reactor and providing a carrier gas; (b) performing a low temperature bake cycle on the substrate at approximately 850 degreesC; (c) heating the substrate while providing N+ dopant gas in the carrier gas; (d) **performing** a **high** temperature bake cycle on the substrate in the presence of N+ dopant; (e) depositing a first intrinsic cap layer (36) on the substrate; (f) **performing** a first **high** temperature gas purge cycle; (g) depositing a second intrinsic epitaxial cap layer (37); (h) **performing** a second **high** temperature gas purge cycle; and depositing an N- epitaxial layer (38) having a thickness greater than the thickness of either intrinsic cap layers.

USE - The process is designed to reduce the effect of boron autodoping and to improve the NPN collector doping in the deep portion of the collector region.

ADVANTAGE - The method offers a very good control over the dopant level at the bottom of the NPN collector. It provides a high sped complementary **bipolar/complementary metal oxide semiconductor** (**CMOS**) process in which the **NPN** and **PNP transistors** have similar **performance** characteristics. The method provides an **NPN transistors** with higher Sterling-T, lower collector resistance, and lower collector-to-emitter saturation voltage compared to the prior art. It allows of eliminating an undesirable dip in the dopant concentration profile of the collectors of the **NPN transistors** and allows optimization of the dopant concentration profile of the collectors of the **PNP transistors.**

DESCRIPTION OF DRAWING(S) - The figure a partial view of a wafer after deposition of the two intrinsic epitaxial layers and a lightly doped **N type** epitaxial layer.

Silicon substrate (30)
First intrinsic cap layer (36)
Second intrinsic epitaxial cap layer (37)
N- epitaxial layer (38)
pp; 45 DwgNo 8/8

39/3,AB/7 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009726844
WPI Acc No: 1994-006694/199401
Related WPI Acc No: 1993-126085
XRAM Acc No: C94-002614
XRPX Acc No: N94-005544

Differential doping of floor and walls of sub millimetre trench in **silicon@** semiconductor for **PNP** lateral **transistor** - comprises forming thin oxide layer, implanting P or **N type** impurity, removing oxide layer and diffusing further impurity

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: DIVAKARUNI S; EL-KAREH B; JOHNSON E D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5273913	A	19931228	US 92909938	A	19920707	199401	B
			US 92980155	A	19921123		

Priority Applications (No Type Date): US 92909938 A 19920707; US 92980155 A 19921123

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5273913	A		6	H01L-021/265	Div ex application US 92909938 Div ex patent US 5198376

Abstract (Basic): US 5273913 A

Differential doping of the floor and walls of a sub-millimetre trench in a **Si** semiconductor surface is carried out by: (a) providing a thin oxide layer on the walls and floor; (b) implanting a p- or **n-type** impurity into the floor by vertical ion implantation through the oxide layer; (**c**) removing the oxide layer; and (d) diffusing another p- or **n-type** impurity into the walls.

Pref. both the walls and the floor are doped with phosphorus, the doping being heavier in the floor than in the walls. The walls are doped by open tube diffusion. The trench is sub-micron.

USE/ADVANTAGE - The process is used in the production of a **pnp** lateral **transistor** in a semiconductor substrate. It allows production of a **high performance pnp** lateral **transistor** and is compatible with **BiCMOS** technology.

Dwg.3/4

39/3,AB/8 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003905076
WPI Acc No: 1984-050621/198409
XRAM Acc No: C84-021182
XRPX Acc No: N84-038292

Contacting narrow PN junction regions in integrated circuits - using narrow vertical conductor to form region and connect it with horizontal conductor

Patent Assignee: IBM CORP (IBMC)
Inventor: BHATIA H S; BHATIA S S; RISEMAN J; VALSAMAKIS E A
Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 100897	A	19840222	EP 83106872	A	19830713	198409	B
JP 59034661	A	19840225	JP 83109464	A	19830620	198414	
US 4507171	A	19850326	US 82405844	A	19820806	198515	
US 4712125	A	19871208	US 84661999	A	19841018	198751	
EP 100897	B	19890419				198916	
DE 3379699	G	19890524				198922	

Priority Applications (No Type Date): US 82405844 A 19820806

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 100897	A	E	24		
	Designated States (Regional): DE FR GB				
EP 100897	B	E			
	Designated States (Regional): DE FR GB				

Abstract (Basic): EP 100897 A

Contact is made by (a) forming an insulating layer on a first type surface region (14) of a monocrystalline semiconductor body; (b) forming a conductive layer over the insulator; (c) etching regions of conductive and insulating layers to the **Si** body, forming horizontal and vertical surfaces; (d) forming a conformal conductor layer on the surfaces; (e) etching the conformal conductor to remove horizontal portions, providing a narrow vertical conductive layer on vertical surfaces and body; (f) forming an insulating layer over the surfaces; (g) heating to diffuse second type dopant into the body from the vertical conductor, forming a narrow width pn junction region; and (h) forming an electrical contact to the conductive layer through the insulator, contacting the junction region via the vertical conductive layer. An IC body having the structure resulting from the above process is claimed. The junction **regions** are pref. **emitter** (46) and collector (44) of a lateral **pnp transistor.**

Contact to narrow junction regions can be made at any convenient region of the upper surface.

6/13

Abstract (Equivalent): EP 100897 B

A method for making contact to one or more narrow width PN junction forming regions comprising: providing a monocrystalline semiconductor body whose at least surface region is of a first conductivity type, forming an insulating layer on said surface region; forming a conductive

layer over said insulating layer; etching regions of said conductive layer and said insulating layer down to said surface region to form substantially horizontal surfaces and substantially vertical surfaces on the layered structure; forming a conformal conductive layer containing a dopant of a second conductivity type over said substantially horizontal surfaces and said substantially vertical surfaces; etching said conformal conductive layer to substantially remove it from said horizontal surface and to leave behind a narrow vertical conductive layer (26) upon said substantially vertical surfaces and said surface region of said semiconductor body; forming an insulator over said conductive layer and said narrow vertical conductive layer; heating said body and said layered structure to a temperature to cause the dopant of the second conductivity type to diffuse into said body from said narrow vertical conductive layer to form said narrow width PN junction forming region and forming an electrical contact to said conductive layer through said insulator which effectively contacts said narrow width PN junction forming region through said conductive layer and said narrow vertical conductive layer.

(12pp)

Abstract (Equivalent): US 4712125 A

Integrated circuit has a semiconductor body with surface regions separated by a pattern of isolation. A narrow pn junction is in at least one of the surface regions and has a width equally that of its contact. A vertical conformal conductive layer (26) of submicron thickness is in the contact. A horizontal conductive layer (22) is in electrical contact with an upper vertical edge of the vertical layer and is separated from the surface regions by an insulating layer (28).

The horizontal layer is thicker than the vertical one. There is an insulating layer over the horizontal layer. A contact to the horizontal layer through an opening in the second insulating layer contacts the pn junction through the horizontal and vertical layers.

USE/ADVANTAGE - Highly dense integrated circuits mfr.. **High performance** circuits are obtd..

(10pp)
US 4507171 A

In making contact to a narrow pn junction in a semiconductor an insulating layer (20) is formed on a monocrystalline substrate followed by forming a conductive layer (22).

The layers are etched to form horizontal and vertical surfaces on the layered structure and a conformal conductive layer (26) formed on these surfaces.

The horizontal conductive layer is etched away and an insulator (28) formed over the conductive layer and vertical conformal layer.

The assembly is heated to diffuse dopant from the conformal layer into the body to form the pn junction.

An electrical contact is formed to the conductive layer through the insulator.

USE/ADVANTAGE - Very dense **high performance** bipolar integrated circuit.

(9pp

39/3,AB/9 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06482710
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 2000-068288 [JP 2000068288 A]
PUBLISHED: March 03, 2000 (20000303)
INVENTOR(s): KURANOUCHI ATSUSHI
APPLICANT(s): SONY CORP
APPL. NO.: 10-325188 [JP 98325188]
FILED: November 16, 1998 (19981116)
PRIORITY: 10-159224 [JP 98159224], JP (Japan), June 08, 1998 (19980608)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **high-performance high**-reliability semiconductor device in which a **MOS** transistor and a bipolar transistor(s) of double-**polysilicon** structure are consolidated, by forming the collector electrode of a transistor with a stacking composite of a first conductive film, a barrier metal film, and a second conductive film.

SOLUTION: This semiconductor device is constituted by an **n-type** epitaxial layer 103 formed on a **p-type silicon** semiconductor substrate 101 in which **n-type** buried diffused layers 102 and a device isolation region on its upper layer are formed, while an **NPN transistor** consisting of base, emitter and collector, an L-PNP consisting of emitter, collector and base, and an **N-MOS** transistor, are formed on the surface of the semiconductor substrate. The collector electrode of the **NPN transistor** and the base electrode of the L-**PNP transistor** are made of a stacking composite 123c, 123f of a **polysilicon** film 109b, 109c, a barrier metal layer and an aluminum wiring film, respectively, wherein the **polysilicon** film 109 is composed of the same conductive material as that of the gate electrode of the **N-MOS** transistor.

39/3,AB/10 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06398589
LATERAL TRANSISTOR AND ITS MANUFACTURE

PUB. NO.: 11-340242 [JP 11340242 A]
PUBLISHED: December 10, 1999 (19991210)
INVENTOR(s): KINOSHITA YASUSHI
APPLICANT(s): MITSUBISHI ELECTRIC CORP
APPL. NO.: 10-141476 [JP 98141476]
FILED: May 22, 1998 (19980522)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **high-performance** lateral **PNP transistor** which is capable of improving its current amplification factor and providing a good contact, and a method for manufacturing the transistor.

SOLUTION: A recess 20 is made in an **N-type** epitaxial layer 4 through anisotropic etching, and a **P-type** collector diffused layer 9 and a **P-type emitter** diffused layer 10 are formed recessed by oblique rotating ion implantation 19 or by diffusion from a doped **polysilicon** 22. Thereafter, silicides are formed on the bottom and side surfaces of the recess 20.

42/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7223279 INSPEC Abstract Number: B2002-05-2570K-001
Title: Minimizing thermal resistance and collector-to-substrate capacitance in **SiGe BiCMOS** on SOI
Author(s): Mastrapasqua, M.; Palestri, P.; Pacelli, A.; Celler, G.K.; Frei, M.R.; Smith, P.R.; Johnson, R.W.; Bizzarro, L.; Lin, W.; Ivanov, T.G.; Carroll, M.S.; Kizilyalli, I.C.; King, C.A.
Author Affiliation: Agere Syst., Murray Hill, NJ, USA
Journal: IEEE Electron Device Letters vol.23, no.3 p.145-7
Publisher: IEEE,
Publication Date: March 2002 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
SICI: 0741-3106(200203)23:3L.145:MTRC;1-2
Material Identity Number: I338-2002-004
U.S. Copyright Clearance Center Code: 0741-3106/02/$17.00
Language: English
Abstract: We describe a low fabrication cost, **high-performance** implementation of **SiGe BiCMOS** on SOL The use of high-energy implant allows the simultaneous formation of the subcollector and an additional **n-type** region below the buried oxide. The combination of buried oxide layer and floating **n-type** region underneath results in a very low collector-to-substrate capacitance. We also show that this process option achieves a much lower thermal resistance than using SOI with deep trench isolation, both reducing cost and curbing self-heating effects.
Subfile: B

42/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7176081 INSPEC Abstract Number: B2002-03-2560J-016
Title: **High performance** 0.25 mu m **SiGe** and **SiGe:C** HBTs using non selective epitaxy
Author(s): Baudry, H.; Martinet, B.; Fellous, C.; Kermarrec, O.; Campidelli, Y.; Laurens, M.; Marty, M.; Mourier, J.; Troillard, G.; Monroy, A.; Dutartre, D.; Bensahel, D.; Vincent, G.; Chantre, A.
Author Affiliation: Centre Commun. de Microelectronique de Crolles, ST Microelectron., Crolles, France
Conference Title: Proceedings of the 2001 BIPOLAR/BiCMOS Circuits and Technology Meeting (Cat. No.01CH37212) p.52-5
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA 199 pp.
ISBN: 0 7803 7019 8 Material Identity Number: XX-2001-02296
U.S. Copyright Clearance Center Code: 0-7803-7019-8/01/$10.00
Conference Title: Proceedings of the 2001 BIPOLAR/BiCMOS Circuits and Technology Meeting
Conference Sponsor: IEEE Electron. Devices Society; IEEE Solid-State Circuits Society; IEEE Twin Cities Sect
Conference Date: 30 Sept.-2 Oct. 2001 Conference Location: Minneapolis, MN, USA
Language: English
Abstract: A robust 0.25 mu m double-poly **SiGe** HBT structure using non selective epitaxy has been developed. The device features 70/90 GHz f/sub T//f/sub max/ with pure **SiGe** base in 0.25 mu m **BiCMOS**

technology. Performances up to 120/100 GHz f/sub T//f/sub max/ are demonstrated for **SiGe:C** base transistors.
Subfile: B

42/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

04111470 INSPEC Abstract Number: B9204-2570K-010
Title: A CRYO-**BiCMOS** technology with **Si/SiGe** heterojunction bipolar transistors
Author(s): Imai, K.; Yamazaki, T.; Tashiro, T.; Tatsumi, T.; Niino, T.; Aizaki, N.; Nakamae, M.
Author Affiliation: NEC Corp., Kanagawa, Japan
Conference Title: Proceedings of the 1990 Bipolar Circuits and Technology Meeting (Cat. No.90CH2890-2) p.90-3
Editor(s): Jopke, J.
Publisher: IEEE, New York, NY, USA
Publication Date: 1990 Country of Publication: USA 262 pp.
Conference Sponsor: IEEE
Conference Date: 17-18 Sept. 1990 Conference Location: Minneapolis, MN, USA
Language: English
Abstract: A **high-performance** liquid-nitrogen temperature **BiCMOS** (CRYO-**BiCMOS**) technology with **Si/SiGe** heterojunction bipolar transistors (HBTs) is presented. The newly developed HBT, which has an n/sup +/-**polysilicon/n-type Si** epitaxial layer emitter structure on a **p-type SiGe** base layer, shows a high current gain of 50 at liquid nitrogen temperature. Under the conditions of 3.3 V and 83 K, the driving capability of CRYO-**BiCMOS** gates is two times larger than that of the CRYO-**CMOS** gate. At 3.3 V and a load capacitance of 1 pF, the gate delay of CRYO-**BiCMOS** gate with pull-up HBT is 480 ps. The CRYO-**BiCMOS** with **Si/SiGe** HBTs presented is very promising for the future progress of **BiCMOS** LSIs.
Subfile: B

42/3,AB/4 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06447123
E.I. No: EIP03297544958
Title: 2D-simulation and analysis of lateral SiC **N-emitter SiGe P**-base Schottky metal-collector (NPM) HBT on SOI
Author: Kumar, M. Jagadesh; Reddy, C. Linga
Corporate Source: Department of Electrical Engineering Indian Inst. of Technology, Delhi, Hauz Khas, New Delhi 110 016, India
Source: Microelectronics Reliability v 43 n 7 July 2003. p 1145-1149
Publication Year: 2003
CODEN: MCRLAS ISSN: 0026-2714
Language: English
Abstract: We report a novel **BiCMOS** compatible lateral SiC **N-emitter, SiGe P**-base Schottky metal-collector NPM HBT on SOI. The proposed lateral NPM HBT performance has been evaluated in detail using 2-dimensional device simulation by comparing it with the equivalent NPN HBT and homojunction **silicon** NPM BJT structures. Based on our

simulation results, it is observed that while both the lateral NPM and NPN HBTs exhibit high current gain, high cut-off frequency compared to the homojunction NPN BJT, the lateral NPM HBT has the additional benefit of suppressed Kirk effect and excellent transient response over its counterpart lateral **NPN** HBT. The improved **performance** of the proposed NPM HBT is discussed in detail and a **CMOS** compatible process is suggested for its fabrication. 26 Refs.

42/3,AB/5 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015836492
WPI Acc No: 2003-898696/200382
XRAM Acc No: C03-255460
XRPX Acc No: N03-717203
Gate array cell for very large scale integration **silicon** on insulator devices, comprises diffusion regions, and P- and **N-types metal oxide semiconductor** transistors of identical dimensions formed in respective diffusion regions
Patent Assignee: BANSAL J P (BANS-I); BAE SYSTEMS INFORMATION & ELECTRONIC SYS (BRAX)
Inventor: BANSAL J P
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030178648	A1	20030925	US 2002367429	P	20020325	200382 B
			US 2002325030	A	20021219	
US 6765245	B2	20040720	US 2002367429	P	20020325	200448
			US 2002325030	A	20021219	

Priority Applications (No Type Date): US 2002367429 P 20020325; US 2002325030 A 20021219
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030178648	A1		21	H01L-027/10	Provisional application US 2002367429
US 6765245	B2			H01L-027/10	Provisional application US 2002367429

Abstract (Basic): US 20030178648 A1
Abstract (Basic):
NOVELTY - A gate array cell comprises:
(i) P+ diffusion regions formed in an N-well region;
(ii) **P-type metal oxide semiconductor** (**PMOS**) transistors of identical dimensions, which are formed in at least some of the P+ diffusion regions;
(iii) N+ diffusion regions formed on a **p-type** of wafer/chip substrate; and
(iv) **N-type MOS** (**NMOS**) transistors of identical dimensions formed in each of the N+ diffusion regions.
DETAILED DESCRIPTION - A gate array cell comprises:
(a) P+ diffusion regions (20a-**c**) formed in an N-well region (15), where at least some of the P+ diffusion regions are separated from other P+ diffusion regions by a **silicon** oxide layer;
(b) **P-type metal oxide semiconductor** (**PMOS**) transistors (41-46) of identical dimensions, which are formed in at least some of the P+ diffusion regions;
(**c**) N+ diffusion regions (24a-**c**) formed on a **p-**

type of wafer/chip substrate, where the N+ diffusion regions are each separated from at least one of the other N+ diffusion regions by a **silicon** oxide layer; and

(d) **N-type MOS** (**NMOS**) transistors of identical dimensions formed in each of the N+ diffusion regions.

USE - The gate array core cell is used for very large scale integration (VLSI) ASIC (sic) devices. It is also used with a design consisting of SOS (sic), **silicon** on insulator (SOI), **BICMOS** (sic), or GAAS (sic) gate array ASIC designs (claimed).

ADVANTAGE - The core cell is highly flexible and has been analyzed to interconnect all types of logic and memory functions needed for ASIC (sic) designs. The layout of the transistors, pre-wiring of the strategic transistors at **polysilicon** level or at local interconnect level, and the embedded **polysilicon** or local interconnect wires reduce the core cell size. The core cell design reduces the overall wiring lengths, parasitic capacitance, which in turn reduce delays, power dissipation and increase ASIC (sic) performance and circuit density. Gate array ASIC (sic) components designed using the core cell provide circuit density, performance and power dissipation characteristics comparable to the standard cell ASICs (sic) but with the advantage of reducing the mask cost and processing time by 50%.

DESCRIPTION OF DRAWING(S) - The figure illustrates the design of the gate array core cell.

N-well region (15)

P+ diffusion regions (20a-**c**)

N+ diffusion regions (24a-**c**)

Transistors (41-46)

pp; 21 DwgNo 2/12

42/3,AB/6 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

009611145

WPI Acc No: 1993-304693/199339

XRAM Acc No: C93-135590

XRPX Acc No: N93-234379

Thin-film pseudo-planar poly-**silicon**@ gate P-**FETs** - formed simultaneously with bulk P-PET and N-**FET** devices in a **CMOS** or **BICMOS** semiconductor structure and useful for load devices in 6D SRAMS

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)

Inventor: CEDERBAUM C; CHANCLOU R; COMBES M; MONE P

Number of Countries: 005 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 562207	A1	19930929	EP 92480048	A	19920327	199339	B
JP 6013582	A	19940121	JP 9328725	A	19930218	199408	
US 5320975	A	19940614	US 9334325	A	19930322	199423	
EP 562207	B1	19960605	EP 92480048	A	19920327	199627	
DE 69211329	E	19960711	DE 611329	A	19920327	199633	
			EP 92480048	A	19920327		

Priority Applications (No Type Date): EP 92480048 A 19920327

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 562207	A1	E	24	H01L-021/82	
JP 6013582	A		21	H01L-027/11	

US 5320975 A 19 H01L-021/70
EP 562207 B1 E 23 H01L-021/82
Designated States (Regional): DE FR GB
DE 69211329 E H01L-021/82 Based on patent EP 562207

Abstract (Basic): EP 562207 A

A method is disclosed for forming thin-film pseudo-planar poly-**Si** gate PFETs (pPFETs) simultaneously with bulk PFET and NFET devices in a **CMOS** or Bi **CMOS** semiconductor structure, including: a) forming several isolation regions (28) in the upper surface of a **p-type Si** substrate (23); b) delineating **Si** lands (32A) above certain isolation regions (28E); **c**) forming N-well regions (35) in the substrate (23) where bulk PFETs are to be formed; d) forming insulator-encapsulated conductive poly-**Si** studs (39A, etc.) to be used as gate electrodes at chosen locations; e) forming self-aligned source/drain regions (52) of the bulk PFETs and pPFETs in the substrate and poly-**Si** lands respectively; and f) forming contact regions (53) to desired locations including the source/drain regions.

USE/ADVANTAGE - Method is partic. applicable to poly-**Si** PFETs used as load devices in six-device (6D) SRAM cells. The process is compatible with any standard **CMOS** process. Complexity and cost are reduced due to the many common steps between fabrication of the bulk **FETs** and the pPFETs.

Dwg.4A/7

Abstract (Equivalent): EP 562207 B

A method of forming thin film pseudo-planar **polysilicon** gate PFETs (pPFETs) simultaneously with bulk PFET and NFET devices in a **CMOS** or BiC-**MOS** semiconductor structure including the steps of (a) elaborating a **P type silicon** substrate (23) having a major surface provided with a plurality of isolation regions (28) as the initial structure, (b) delineating **polysilicon** lands (32A) above certain isolation regions (28E), (**c**) forming N-well regions (35) into the substrate (23) where bulk PFETs are to be subsequently formed, (d) forming insulator encapsulated conductive **polysilicon** studs (39A,B,**C**,D,E) to be used as gate electrodes of the pPFETs and bulle PFET and NFET devices at desired locations of the structure, (e) forming source/drain regions (50) of the bulk NFETs into the substrate self-aligned to the **polysilicon** studs, (f) forming source/drain regions (52) of the bulk PFETs and pPFETs into the substrate and **polysilicon** lands respectively self-aligned to the **polysilicon** studs, and (g) forming contact regions (53) to the desired locations including the source/drain regions.

(Dwg.4/7

Abstract (Equivalent): US 5320975 A

Thin film pseudo-planar **polysilicon** gate PFET's (pPFET's) simultaneously with bulk PFET and NFET devices in a **CMOS** or **BICMOS** structure using a **P-type silicon** substrate with multiple isolation regions. **Silicon** lands are delineated at selected locations and N-wells formed in locations where bulk PFET's are to be located. Encapsulated **silicon** studs at selected locations form gate electrodes. Self aligning source/drain regions are formed in the bulk NFET'S followed by self aligning source/drain regions into the substrate. Finally contact regions are formed at selected locations into the substrate.

USE/ADVANTAGE - Load devices in 6D scram cells. Dense **high performance** devices can be more readily fabricated.

(Dwg.7/7